VNIVERSITAT DE VALÈNCIA

Course Guide
44280 Hardware systems of signal processing

COURSE DATA

Data Subject	
Code	44280
Name	Hardware systems of signal processing
Cycle	Master's degree
ECTS Credits	3.0
Academic year	2020 - 2021

Study (s)

Degree	Center	Acad. year	Period
2199 - M.D. in Electronic Engineering	School of Engineering	1	Second term

Subject-matter

Degree	Subject-matter	Character
2199 - M.D. in Electronic Engineering	1 - Digital signal processing	Obligatory

Coordination

Name	Department
BATALLER MOMPEAN, MANUEL	242 - Electronic Engineering

SUMMARY

The course Hardware Systems Signal Processing is part of the treatment field Digital Signal whose credits range from data processing techniques to implementation in hardware real time systems.

The content of this field is organized in 5 subjects with compulsory charge, each of 3 credits ECTS and can be grouped into three thematic blocks. The first section focuses on introducing techniques for exploratory data analysis, the second describes advanced techniques of digital signal processing and the third focuses on the physical implementation of such systems with a special emphasis on its implementation in real time.

The subject of this guide is mandatory, four-monthly and is taught in the Masters degree in Electrical Engineering. The curriculum consists of a total of 3 ECTS credit.

Once they have been described in other subject matter Digital Processing of advanced techniques signals digital signal processing, among which may be mentioned spectral estimation, prediction techniques of time - frequency analysis and design of linear filters and nonlinear linear adaptive filters, etc. implementation arises in physical systems. To this end, this course needs calculation and memory techniques described will be analyzed and design techniques specific digital systems will be described, such as FPGA and System on Chip. Attention to high-level hardware synthesis will be given, including

the most used software tools such as VHDL, Verilog, System Generator, AccelDSP , SystemC , Handel-C , etc. . Technical hardware-software co-design and integration of functional modules in FPGA partitioning and fundamentals of software / hardware design and simulation and test of complex systems will be studied. Practices on programmable logic devices FPGA will be made, making the description in VHDL or other hardware description languages algorithms digital signal processing. Finally, the synthesis and physical implementation will take place in different Xilinx development boards.

The content must give students a set of skills that allow you to design and materialize a physical device in high-level descriptions of algorithms for digital signal processing.

The objectives of this course are summarized in the following points:

- Various types of hardware devices that are on the market addressing an electronic design.
- Select the most appropriate type of hardware design as needed.
- Ask the theoretical design of an electronic system that meets a set of functional specifications.
- To design each of the subsystems that compose it. Construct the corresponding algorithm in the form of pseudocode.
- Optimize the computational units to be used depending on the system requirements (low resource consumption or high performance).
- Perform VHDL and / or Verilog algorithm of digital signal processing description and corresponding simulation.
- Perform the description of an algorithm using digital signal processing hardware description languages based on C.
- Perform the description of an algorithm using the PDS System Generator from Xilinx and / or AccelDSP tools.
- Develop systems for data exchange between the device and designed A / D and D / A.
- Perform physical implementation using programmable devices and verify their actual performance.
- Addressing projects in which they are involved various types of electronic devices for the design of interconnection between them and develop the necessary programming to perform a specific function.
- Adequately resolve the limitations calculating arithmetic in hardware devices without affecting the proper functioning of the hardware system.

The contents of the course are:

- Programmable Digital Systems: FPGA. Systems on Chip (SoC). Applications and types.

- Hardware description languages.
- Hardware description languages based on C.
- Tools for high-level description.
- Hardware design techniques for signal processing algorithms

PREVIOUS KNOWLEDGE

Relationship to other subjects of the same degree

There are no specified enrollment restrictions with other subjects of the curriculum.

Other requirements

Successfully addressing this subject is recommended that the student possesses prior knowledge acquired in the subjects of Electronic Circuits and Digital Systems I, II, Signals and Linear Systems and Digital Signal Processing. Such prior knowledge include:

Numbering Systems
Boolean algebra
Maxterms, minterms and a logic function.
Simplification of logical functions: Karnaugh methods and Quine-McCluskey
Combinational and Sequential Subsystems.
Design of state machines.
Sampling and reco

OUTCOMES

2199 - M.D. in Electronic Engineering

- Capacidad para proyectar, calcular y diseñar productos, procesos e instalaciones en todos los ámbitos de la Ingeniería Electrónica y en particular los de tratamiento de la señal, sistemas digitales y de comunicaciones y electrónica industrial.
- Capacidad para el modelado matemático, cálculo y simulación en todos los ámbitos relacionados con la Ingeniería Electrónica y campos multidisciplinares afines. En especial los de tratamiento de la señal, sistemas digitales y de comunicaciones y electrónica industrial.
- Capacidad de analizar, especificar y diseñar sistemas de tratamiento digital de señales desde su concepción hasta su implementación en sistemas hardware de tiempo real..

LEARNING OUTCOMES

Learning outcomes of the course are:

1. Knowledge and use of Programmable Digital Systems (FPGA) .
2. Knowledge and ability to use System -on-Chip (SoC).
3. Knowledge and application of the basics of hardware description languages devices.
4. Knowledge and application of the basics of hardware description languages based devices C.
5. Manage tools high level description .
6. Apply digital technologies for problem solving and applications in various fields of application, especially in the implementation of algorithms for digital signal processing .
7. Understand and manage hardware design techniques .
8. Being able to tackle projects that they are involved various types of electronic devices for the design of interconnection between them and develop the necessary programming to perform a specific function .
9. Understand and know how to use basic and advanced techniques of digital signal processing applied to real time.

DESCRIPTION OF CONTENTS

1. PROGRAMMABLE DIGITAL SYSTEMS

FPGA devices description of. Introduction to systems on chip (SoC).

2. ALGORITHMIC STATE MACHINE DESIGN

ASM design methodology. VHDL description of control unit. VHDL description of datapath.

3. VHDL HARDWARE DESCRIPTION LANGUAGE

Introduction and justification for the high-level languages: VHDL. Components. Sequential and concurrent statements. Testbench. Examples. Synthesis from VHDL: methodology, synthesis of combinational logic and sequential logic.

4. TOOLS HIGH LEVEL DESCRIPTIONS

Introduction to hardware environments High Level Design: System Generator. Xilinx System Generator. Examples.

5. HARDWARE DESCRIPTION LANGUAGES BASED ON C

Introduction. SystemC: language elements, data types, ports. Sentences. Examples.

6. Laboratory Practices

VHDL description of signal processing systems. SystemC description of combinational and sequential subsystems. Tools high level description.

WORKLOAD

ACTIVITY	Hours	% To be attended
Theory classes	15,00	100
Laboratory practices	15,00	100
Readings supplementary material	5,00	0
Preparation of evaluation activities	15,00	0
Preparing lectures	10,00	0
Preparation of practical classes and problem	15,00	0
TOTAL	**75,00**	

TEACHING METHODOLOGY

The development of the course is structured around lectures , tutorials and labs.

In the theory sessions lecture model will be used. To do this, the teacher will present the fundamental contents of the subject using audiovisual means available (presentations, transparencies, blackboard) . The practical classes will develop problems following two models . Some of the classes will be the teacher who solves a number of problems such that students learn to identify the essential elements of the approach and problem resolution. In other kinds of problems that students will be solving similar problems under the supervision of the teacher.

Students have a tutorial schedule whose purpose is to solve problems , doubts, guidance papers, etc. The schedule of these tutorials are indicated in the beginning of the academic year . They will also have the opportunity to clarify some questions via email or forums discussion by using the tool " Virtual Classroom" , which provides the University of Valencia.

The laboratory practice sessions are organized around the design, simulation and implementation on a physical device of a given digital system. Its estimated duration is 3 hours and group practices will consist of two people maximum. Students will have the scripts for practice and testing will be conducted entirely by them under the supervision of the teacher.

May be made during the course some jobs that complement the explanation for the same . The Works consist of complete resolution of a real project or other proposals that the teacher deems appropriate.

The e-learning platform (Virtual Classroom) of the University of Valencia will be used to support communication with students. Through it will have access to training materials used in class, as well as problems and exercises to solve.

EVALUATION

Learning theory and the laboratory will be evaluated. To average the marks of theory and laboratory will need to note each of them separately is equal to or greater than 4. The final mark will be obtained from the following considerations:

- The theory mark will emerge as a result of carrying on the dates indicated in the official calendar of the written examination. It will consist of several questions of theoretical and practical. All questions will be related to the contents of the agenda, and with similar issues and problems done in class difficulty.
- The laboratory note arise as a result of the realization of an individual at the end of the semester will consist of the design, simulation and implementation on a physical examination of a digital system. Demonstrated skill, proficiency in the use of laboratory equipment and design development throughout the session will be assessed.
- Finally, in case that work it will have a weight of 25% is performed.

If any work will be done the percentages would be:

- 40% theory exam
- 30% laboratory test
- 25% work
- 5% Attendance

The percentages in the case of not doing any work are:

- 55% theory exam
- 45% laboratory test

“In any case, the evaluation system will be governed by what is established in the Evaluation and Qualification Regulations of the Universitat de València for Degrees and Masters (https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639)”.

REFERENCES

Basic

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- Bhasker, J. A SystemC Primer. Star Galaxy Publishing. 2005
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- Grötker, T.; Liao, S.; Martin, G.; Swan, S. System Design with SystemC. Springer. 2002
- Deschamps, J.P.: "Síntesis de circuitos digitales. Un enfoque algorítmico". Thomson-Paraninfo, 2002

ADDENDUM COVID-19

This addendum will only be activated if the health situation requires so and with the prior agreement of the Governing Council

English version is not available