COURSE DATA

Data Subject	
Code	34882
Name	Digital Systems I
Cycle	Grade
ECTS Credits	6.0
Academic year	2019 - 2020

Study (s)

Degree	Center	Acad. year	Period
1403 - Degree in Telematics Engineering	School of Engineering	2	First term

Subject-matter

Degree	Subject-matter	Character
1403 - Degree in Telematics Engineering	9 - Digital electronic systems	Obligatory

Coordination

Name	Department
PARDO CARPIO, FERNANDO	240 - Computer Science

SUMMARY

Name of subject: Digital Electronic Systems I

Number of ECTS credits: 6

Temporary location: Second year, first semester

Subject: Digital Electronic Systems

Character: Mandatory

Qualification: Telematics Engineering

Cycle: Degree

Department: Computing

Teachers responsible: Pardo Fernando Carpio

Introduction

The Digital Electronic Systems I course is part of the material of the same name whose overall goal is to teach the basic techniques for analysis and synthesis of digital systems, laying the foundation for subsequent courses that facilitate the study of more complex designs.

It is a compulsory subject that is taught quarterly basis in the second year of the degree of Telematics Engineering during the first quarter. The curriculum consists of a total of 6 ECTS. This course provides students with a global and comprehensive digital systems within the field of digital electronic design. The contents should allow a student to approach the design of a digital system being able to analyze an application that requires this type of design. To this end, requires knowledge of the various existing digital subsystems (subsystems combinational, sequential, timing, etc..), Programmable logic devices and their operation and design.

This is a very practical course in which, following the introduction of the concepts, students will undertake numerous practical exercises, mainly from analysis and design of digital systems, as well as laboratory experimentation.

In short, this course offers an overview of the techniques of analysis and design of digital electronic circuits and systems.

General Objectives

The purpose of this course is to give students a set of knowledge, skills and competencies, both on the grounds and on the basic components that make up a digital system. Also we study the logical design methodology, so that students can undertake the analysis and design, both combinational and sequential systems, integrated circuits using SSI and MSI technology and programmable logic devices. Finally, they must be able to understand the existing commercial solutions and know how to treat them properly.

PREVIOUS KNOWLEDGE

Relationship to other subjects of the same degree

There are no specified enrollment restrictions with other subjects of the curriculum.

Other requirements

Successfully addressing this subject is recommended that the student has previous knowledge of digital electronics that must be acquired in the course of Circuits scheduled in the first year of this degree. Among such prior knowledge include:

Numbering systems
Boolean algebra
Maxterms minterms and a logic function.
Simplification of logical function: methods of Karnaugh

OUTCOMES

1403 - Degree in Telematics Engineering

- R9 - Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous, and use microprocessors and integrated circuits.
- G3 - Acquisition of the knowledge of the basic and technological subjects that allows students to learn new methods and theories and endows them with the versatility to adapt to new situations.
- G4 - Ability to solve problems with initiative, decision-making and creativity, and to communicate and transmit knowledge, abilities and skills, understanding the ethical and professional responsibility of the activity of a telecommunications technical engineer.
- R10 - Understand and apply the fundamentals of hardware description languages describing hardware devices.

LEARNING OUTCOMES

Learning outcomes of field of Digital Electronic Systems are:

1. Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous. (R9)

2. Capacity for analysis and design of digital circuits using SSI and MSI integrated circuits. (R9, R10)

3. Ability to design digital electronic systems. (R9, R10)

4. Applying digital technology to solve problems and applications in various fields of application. (R9, R10)

5. Properly plan the overall structure of a digital system and the interrelationship between its various elements. (R9, R10, G3, G4)

6. Manage the design and programming tools necessary to enable the smooth operation of a digital system. (R9, R10, G3, G4)

7. Select simple programmable logic devices. (R9, R10)

8. Knowledge and application of the fundamentals of description languages hardware devices. (R10, G3, G4)

9. Program and simulate the behavior of digital systems using hardware description language. (R10, G3, G4)

The student must be able to:

- Knowing the design methodology of digital systems.
- Learn the methodology of analysis of digital systems.
- Know the basic combinational subsystems (circuits encoders, multiplexers, comparators, etc..).
- To know the basic sequential subsystems (flip-flops, registers, counters, etc..).
- Knowing the timing and clock circuits.
- Gain experience in assembling and testing of digital circuits.
- Gain experience in using circuit simulation tools and electronics.
- Knowing programmable logic devices.
- Understanding the basics of hardware description languages.
- Program and simulate the behavior of digital systems using hardware description language (HDL).
- Make designs that meet a set of specifications using devices SSI, MSI and programmable logic.
- Work together to plan the realization of a design dividing the workload and thus address complex problems.

In addition to the specific objectives mentioned above, during the course will encourage the development of several generic skills, among which include:

- Ability to apply the scientific method of experimental resolution.
- Capacity for analysis and synthesis.
- Ability to argue from rational and logical criteria.
- Ability to communicate properly and organized.
- Ability to develop a problem in a systematic and organized.
- Ability to build a comprehensive and organized written document that defines a project.
- Capacity for personal work and timing.
- Ability to work in groups.
- Ability to manage information.

DESCRIPTION OF CONTENTS

1. Design Methodology

Design flow. Design specification. Hierarchical Design. Schemes. Hardware Description Languages. Simulation. Automatic Synthesis. Introduction to VHDL. Entity and Architecture. Examples.

2. Combinational Circuits

Analysis and synthesis. Implementation. Logical risks.

3. MSI combinational blocks

Encoders, Decoders. Multiplexers, demultiplexers. Compare ers. Arithmetic Logic Unit.

4. Sequential Circuits

Flip-flops. Latches and flip-flops. Sequential SSI / MSI. Timing. Clock circuits.

5. State machines

State machine definition. Synthesis of state machines. Temporal analysis.

6. Programmable Logic

Simple devices. Complex programmable logic. FPGAs.

WORKLOAD

ACTIVITY	Hours	% To be attended
Theory classes	30,00	100
Laboratory practices	20,00	100
Classroom practices	10,00	100
Development of group work	20,00	0
Development of individual work	15,00	0
Study and independent work	25,00	0
Readings supplementary material	5,00	0
Preparation of evaluation activities	10,00	0
Preparing lectures	5,00	0
Preparation of practical classes and problem	10,00	0
TOTAL	**150,00**	

TEACHING METHODOLOGY

The training activities are conducted in accordance with the following distribution:

40% of load hours the student will go to the following classroom activities:

- **Theoretical activities.**

Description: In the theoretical issues will be developed to provide a global and inclusive, analyzing in detail the key issues and more complex, promoting at all times, participation / student. (R9, R10, G3, G4)

- **Practical activities.**

Description: Complementing the theoretical activities in order to apply the basic concepts and extend them with knowledge and experience they acquire during the course of the work proposed. They include the following types of classroom activities:

or Classes of problems and issues in the classroom (G3, G4)

or Discussion sessions and problem solving exercises and previously worked by students (R9, R10, G3, G4)

or Lab (R9, R10, G3, G4)

or Tutorials (individual or group)

- **Evaluation.**

Description: Performing individual evaluation questionnaires in the classroom with the presence of teachers.

60% of load hours the student will focus on the following activities to be considered:

- **Personal work of students.**

Description: Carrying out of the classroom issues and problems, and the preparation of classes and exams (study). This task is done individually and tries to promote self-employment. (R9, R10, G3, G4)

- **Working in small groups.**

Description: Conduct, by small groups of students (2-4) of work, issues, problems outside the classroom. This work complements the individual and promotes the ability to integrate into working groups. (R9, R10, G3, G4)

The percentage of approximate workload of each of the sections mentioned above is shown in the following table.

Paragraph	**Loading percentage**
Theoretical activities	17%
Practical Activities	20%
Evaluation	3%
Personal work of students	45%
Work in small groups	15%

TOTAL 100%

It uses the platform of e-learning (virtual classroom) from the University of Valencia in support of communication with students. Through it we have access to learning materials used in class as well as to solve problems and exercises.

EVALUATION

Note that this text is the result of a translation from the original in Spanish. If there are differences in meanings among versions, the good meaning is the one found in the original version in Spanish.

The evaluation of the course will be held on the first call by:

• Continuous assessment based on participation and degree of involvement in the teaching-learning process, given regular attendance and classroom activities provided for resolution of issues and problems raised. This part, called P, shall consist of the following parts:

or Attendance and class delivery by the student, individually or in groups, exercises and questions raised in preparation or is do the sessions. **The student must have attended and/or delivered to least 80% of these jobs to score in this part. We can not approve on first call the subject if not submitted at least 60% of the proposed work.**

or Class participation in solving problems through the Forum or the subject responding to the issues raised.

• Individual objective tests, consisting of several tests or knowledge tests, which consist of both theoretical and practical issues as problems to be undertaken in the first half of the semester (called T1), during the second half of the semester (T2) and out of teaching time in the examination period (called T3). The distribution of each individual test of T is as follows:

$$T = 0.15 * T1 + 0.3 * T2 + 0.55 * T3$$

Each of these tests will address all of the subject content taught so far.

• Evaluation of laboratory practice activities (L) from the achievement of objectives in the lab sessions, preparation of papers / reports, and conducting preparatory work prior to them. These activities are carried out individually and / or groups as indicated.

The note of the subject (NA) on the first call will be formed as the sum of the previous parts as follows:

$$NA = 0.10 * P + 0.25 * L + 0.65 * \max \{T3, T\}$$

IMPORTANT: If the student has not delivered on time and work part evaluables of P, NA note will be 0 and therefore this first call will be assessed as "not submitted".

In the second call, the students must be submitted to a final exam (FE) and the final (NA) will be computed as:

$$NA1 = 0.10 * P + 0.25 * L + 0.66 * EF$$

$$NA2 = 0.05 * P + 0.20 * L + 0.75 * EF$$

$$NA = \max \{NA1, NA2\}$$

For the L part of the second call, the student may deliver again the lab works that had a fail, or not presented, score in the first call. The new works must be better than those of the first call.

For both calls:

- The delivery of less than 80% of the work requested in the P is P = 0. (The first call will be assessed as "not submitted" if not presented in time at least 60% of the work requested).

- The lack of a laboratory class means that this session will evaluate to 0, unless the absence is justified and submitted documentary work that requires the teacher to his recovery, so be valued less than the present evaluation.

- The absence of over two lab classes implies L = 0, whether justified or not.

- Exceptionally, in duly justified cases prior to the absence, unless prevented, the laboratory class can be retrieved at the time of another group that performs the same practice, in which case will be evaluated as if it had continued on a normal schedule face.

- The values of T or EF should not be less than 3,5 in order to pass. Should the value of these parameters is less than 3,5 the final score will be calculated taking these parameters as 0.

In any case, the evaluation system will be managed by what is written in the "Reglament d'Avaluació i Qualificació de la Universitat de València per a Graus i Màsters" (https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639)

REFERENCES

Basic

- J.F. Wakerly. Diseño digital. Principios y prácticas. 3ª edición. Prentice Hall, 2001
- F. Pardo, J.A. Boluda. VHDL: Lenguaje para síntesis y modelado de circuitos digitales. 3ª edición. Ra-Ma, 2011

Additional

- T.L. Floyd. "Fundamentos de Sistemas Digitales". Prentice Hall, 2007
- J.P. Hayes. "Introducción al Diseño Lógico Digital". Addison-Wesley, 1996
- M. Morris Mano. Diseño Digital. Prentice-Hall, 2003
- S. Alfonso-Pérez, E. Soto, S. Fernández. Diseño de sistemas digitales con VHDL. Thomson-Paraninfo, 2002
- S. Brown and Z. Vranesic. Fundamentals of Digital Logic with VHDL Design. 3ª edición. Mcgraw-Hill (Series in Electrical and Computer Engineering), 2005

ADDENDUM COVID-19

This addendum will only be activated if the health situation requires so and with the prior agreement of the Governing Council

English version is not available