VNIVERSITAT DE VALÈNCIA

Course Guide
34803 Digital Systems I

COURSE DATA

Data Subject	
Code	34803
Name	Digital Systems I
Cycle	Grade
ECTS Credits	6.0
Academic year	2020 - 2021

Study (s)

Degree	Center	Acad. year	Period
1402 - Degree in Telecommunications Electronic Engineering	School of Engineering	1	Second term

Subject-matter

Degree	Subject-matter	Character
1402 - Degree in Telecommunications Electronic Engineering	12 - Digital electronic systems	Obligatory

Coordination

Name	Department
ROSADO MUÑOZ, ALFREDO	242 - Electronic Engineering

SUMMARY

The course ‘Digital Electronic Systems I’ (Sistemas Electrónicos Digitales I) is the first of several courses related to digital electronic systems. The main objective for this course is the study of the basic techniques for the analysis and design of digital systems, setting up the basic knowledge and easing the study of complex systems to be covered in further courses.

This is a compulsory course taught in the first year of the Telecommunication Electronic Engineering degree (GIET) during the second semester (spring semester). This course has a length of 6 ECTS from which 3 ECTS correspond to theory classes, 1 ECTS for problem solving classes and 2 ECTS for laboratory sessions.

This course covers a global vision of digital systems inside the field of digital electronic systems. The proposed topics will allow the student to design a basic digital system and analyse the requirements needed for implementing a digital design. In order to achieve these goals, the students will learn about different digital systems such as combinational and sequential subsystems, timing circuits, basic digital integrated circuits, programmable logic circuits, etc.

This is a practical course. The principles of digital design are accompanied with examples. Students will perform frequent exercises, both for analysis and design of digital systems, which will further test and create in the laboratory.

As a summary, this course provides a basic foundation for design and analysis of digital electronic systems and their associated circuits.

PREVIOUS KNOWLEDGE

Relationship to other subjects of the same degree

There are no specified enrollment restrictions with other subjects of the curriculum.

Other requirements

This course is self-contained and does not require any previous knowledge as it is one of the first courses related to electronics and they do not have previous knowledge in the field.

COMPETENCES (RD 1393/2007) // LEARNING OUTCOMES (RD 822/2021)

1402 - Degree in Telecommunications Electronic Engineering

- G3 - Acquisition of the knowledge of the basic and technological subjects that allows students to learn new methods and theories and endows them with the versatility to adapt to new situations.
- G4 - Ability to solve problems with initiative, decision-making and creativity, and to communicate and transmit knowledge, abilities and skills, understanding the ethical and professional responsibility of the activity of a telecommunications technical engineer.
- Capacidad de análisis y diseño de circuitos combinacionales y secuenciales, síncronos y asíncronos, y de utilización de microprocesadores y circuitos integrados.
- R10 - Understand and apply the fundamentals of hardware description languages describing hardware devices.

LEARNING OUTCOMES (RD 1393/2007) // NO CONTENT (RD 822/2021)

The learning outcomes in the course Digital Electronic Systems are:

1. Ability to design and analyse combinational and sequential circuits, synchronous and asynchronous (R9)

2. Ability to design and analyse digital circuits using standard SSI and MSI circuits (R9)

3. Ability to design digital electronic systems (G3,G4)

4. Apply digital technologies to solve problems and develop solutions based on digital circuits in different fields of application (G3,G4)

5. Adequate planning and conception of the global structure in a digital system and the relations among all different parts of the design (G3,G4,R9)

6. Efficient use of software tools for design and programming of a digital system, allowing the successful design of the system (G3,G4,R9)

7. Selection of digital integrated circuits, including programmable logic devices (G3)

8. Describe a digital function using a Hardware Description Language (R10)

9. Program a digital device and simulate it by means of a Hardware Description Language (R10)

DESCRIPTION OF CONTENTS

1. INTRODUCTION TO DIGITAL ELECTRONIC SYSTEMS

Numeration systems. Binary arithmetic operations. Representation of signed values. Representation of fixed-point values. BCD code. Alphanumeric code types.
Digital Systems: Analysis and Synthesis. Boolean algebra. Simplification of logic functions. Logic Families

2. LOGIC SIMULATOR

Protoboard simulator: introduction, connexions, components. Examples
Logic simulator LTSpice: introduction, libraries, digital stimuli. Examples

3. COMBINATIONAL CIRCUITS

Definition. Analysis and synthesis. Implementation with NAND and NOR gates. XOR and XNOR functions. Multilevel circuits: hazards.

4. INTRODUCTION TO THE HARDWARE DESCRIPTION LANGUAGES

Historical review. Basics. Data Types. Sequential and concurrent instruction. Subprograms. Test benches.

5. MSI CIRCUITS

Encoders and decoders. Code converters. Multiplexers and Demultiplexers. Comparator circuits. Arithmetic circuits. Arithmetic-Logic Units. VHDL description: decoders, multiplexers and arithmetic circuits. Exercises.

6. FLIP-FLOPS CIRCUITS.

RS flip-flop: synchronous and asynchronous operation. JK flip-flop. Master-slave flip-flop. Flip-flop D. Flip-flop T. VHDL description of the Flip-flops. Exercises.

7. INTRODUCCIÓN A LOS CIRCUITOS SECUENCIALES

Definition. Shift registers. Asynchronous counters. Synchronous counters: introduction and design. Types of counters: up-down, ring, Johnson. Examples of circuits MSI. VHDL description of the counters. Exercises.

8. UNITED MACHINE DESIGN

Introduction: Moore and Mealy machines. Analysis of synchronous sequential circuits. Synthesis methodology. VHDL description of Moore machine. Introduction to asynchronous sequential circuits. Exercises

9. DIGITAL CIRCUITS AND CLOCK TIMING

Schmitt Trigger gates. Timer circuits with logic gates. Digital timer circuits. Clock circuits with logic gates. Digital astable circuits.

10. INTRODUCCIÓN A LA LÓGICA PROGRAMABLE

SPLD types and internal block structure: PROM, PAL, PLA, GAL. Design flow. Time Specification. Introduction to CPLDs and FPGA: main manufacturers and their devices.

WORKLOAD

ACTIVITY	Hours	% To be attended
Theory classes	30,00	100
Laboratory practices	20,00	100
Classroom practices	10,00	100
Development of individual work	5,00	0
Study and independent work	30,00	0
Readings supplementary material	5,00	0
Preparation of evaluation activities	10,00	0
Preparing lectures	15,00	0
Preparation of practical classes and problem	14,00	0
Resolution of case studies	10,00	0
Resolution of online questionnaires	1,00	0
TOTAL	**150,00**	

TEACHING METHODOLOGY

The course is organised around three kinds of attending classes: theory class, problem solving class and laboratory class. Office hours are used as additional tool for students. Concerning out-of-classroom activities, additional exercises must be solved, as well as report preparation.

In theory and problem-solving classes, traditional teaching method will be used. In theory sessions the teacher will explain the basic contents of the course using different teaching tools as slide presentation, together with other tools (G3,G4,R9,R10). Problem-solving classes will use two different models. First, the teacher will propose and solve different problems which are essential for proper understanding of digital systems from students, learning to follow a procedure and identify the required elements needed to adequately solve a problem (G3,G4,R9,R10). Second, the teacher will propose a problem and the students must solve the problem being distributed into groups, individually, or using other group working techniques and always under direct supervision of the teacher (G4,R9); once completed, the solutions will be collected by the teacher and corrected by the teacher or the students (depending on the case).

Students have a specific office-hour calendar where the teacher is available in his office for any concern related to the course (problem solving, theory doubts, report guidance, etc.). The attending hours will be detailed at the beginning of the academic year. Additionally, there exist a distance ‘office-hours’ program where questions can be solved using e-mail contact, and it is also promoted the use of the students’ portal ‘Aula Virtual’ provided by the University of Valencia, where all the information related to the course is available online.

Laboratory sessions are organized according to three basic principles: design, mounting (real or virtual mounting) and testing/simulating an electronic digital system (G4,R9,R10). The estimated duration for each laboratory session is 3 hours. The session will be carried out by groups of, at most, two persons. The student will get the laboratory activities' guide in advance so that previous preparation time is allowed. Once in the laboratory, there exists a direct supervision from the teacher. The student must assume the responsibility for all the stages in the proposal: design, mounting and testing. The final goal of the laboratory is to obtain a working system according to initial specifications. Finally, a lab report will be required from the teacher (G3,G4,R9,R10).

All of the described activities will be always using the support of 'Aula Virtual' as the most important source of information and communication for the student.

EVALUATION

Assessment of student learning will take place following two models:

a) By continuous assessment tests from the theoretical sessions and problems, plus the scores obtained in lab sessions. To qualify for this type of evaluation, the student must regularly attend classes and theoretical problems and be active in the dynamics of cooperative work. To average the exam scores of theory and laboratory, it is required that each of them is equal or higher than 4. The final grade is obtained from the following considerations.

- The theory mark will emerge as a result of a written exam, done on the dates indicated in the official calendar for first call. It will consist of different questions of theoretical and practical problems (G3,G4,R9,R10). All questions will be related to the contents of the agenda, and with similar issues and problems done in class difficulty. This classification corresponds to 35% of the final grade (Ex_Teoria).
- Upon completion of the course, a multiple-choice test that will count for 20% of the final grade will be made (G3,G4,R9,R10) (Ex_Test).
- The laboratory note is a result of the realization of an individual exam at the end of the semester, which will include a number of issues directly related to the practices done during the course (G3,G4,R9,R10). It will consist of the design, assembly and / or simulation of some of the sections made by students throughout the laboratory sessions they attended during the course. Demonstrated skills, proficiency in the use of laboratory equipment and design development throughout the session will be assessed. It is a prerequisite to regularly attend lab sessions (you cannot miss more than 1 session). This note is equal to 25% of the final grade (Ex_Lab).
- In addition, each lab sessions is assessed using a few simple questions at the beginning and end of each session (G3,G4,R9,R10). This ongoing evaluation of the work done by students in all lab sessions consider skill, interest and results. This assessment translates into 20% of the final grade for the course (Eval_Lab).

The final grade for the course will come from the following expression:

Final Score = (0,35*Ex_Teoria)+(0,25 * Ex_Lab)+(0,2*Eval_Lab) + (0,2 * Ex_Test)

b) From a single exam to be held on the official date and the grade obtained in laboratory practice sessions . In this mode, the exam will consist of a theoretical part, in which the student must demonstrate knowledge of the concepts and relationships seen in class and a second part which is a laboratory test

(G3,G4,R9,R10). In this, the students must complete the design, assembly and / or simulation of specified digital systems related to the contents of the agenda and with similar issues and practices developed in the laboratory scripts difficulty (G3,G4,R9,R10). To average the test scores of theory and laboratory will require each of them to equal or exceed 4. The final grade for the course will leave the following expression:

Final Score = (0,55*Ex2_Teoria)+(0,25 * Ex2_Lab)+(0,20*Eval_Lab)

Initially, all students will follow evaluation model a), and, in case of failing the course, they will follow model b). In case of partial passing the exams in model a), the student can only repeat the failed exam in the second call. The passed score obtained in model a) will be used to obtain the final score in model b).

The score obtained in laboratory sessions (Eval_Lab) cannot be repeated and the same score will be used for both models.

“In any case, the evaluation system will be governed by what is established in the Evaluation and Qualification Regulations of the Universitat de València for Degrees and Masters (https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639)”.

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Basic

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Additional

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ADDENDUM COVID-19

This addendum will only be activated if the health situation requires so and with the prior agreement of the Governing Council

Contents

The contents initially included in the teaching guide are maintained.

Workload and temporary teaching planning

The different activities described in the teaching guide are maintained with the planned dedication.

The material for the follow-up of the classes of theory/practices allows to continue with the professor of temporary planning so much in days as in schedule, so much if the teaching is face-to-face in the classroom or if it is not.

Teaching methodology

In classroom theory and practices, students will tend to have the maximum physical attendance possible, always respecting the sanitary restrictions that limit the capacity of the classrooms as indicated by the competent public health authorities to the estimated percentage of their usual occupation.

Depending on the capacity of the classroom and the number of students enrolled, it may be necessary to distribute the students into two groups. If this situation arises, each group will attend classroom theory and practical sessions with physical presence in the classroom by rotating shifts, thus ensuring compliance with the criteria for occupying spaces.

The rotation system will be established once the actual enrollment data is known, guaranteeing, in any case, that the attendance percentage of all the students enrolled in the subject is the same.

With respect to laboratory practices, attendance at sessions scheduled in the schedule will be totally face-to-face.

Once the actual enrollment data is available and the availability of spaces is known, the Academic Committee of the Degree will approve the Teaching Model of the Degree and its adaptation to each subject, establishing in said model the specific conditions in which it will be developed teaching the subject.

If there is a closure of the facilities for sanitary reasons that totally or partially affects the classes of the subject, these will be replaced by non-contact sessions following the established schedules.

Evaluation

The evaluation system described in the teaching guide of the subject in which the different evaluable activities have been specified as well as their contribution to the final grade of the subject is maintained.

If there is a closure of the facilities for health reasons that affect the development of any face-to-face evaluable activity of the subject, it will be replaced by a test of a similar nature that will be carried out in virtual mode using the computer tools licensed by the Universitat de València.

The contribution of each evaluable activity to the final grade for the course will remain unchanged, as established in this guide.

Bibliography

The bibliography recommended in the teaching guide.