VNIVERSITAT DE VALÈNCIA

Course Guide
34803 Digital Systems I

COURSE DATA

Data Subject	
Code	34803
Name	Digital Systems I
Cycle	Grade
ECTS Credits	6.0
Academic year	2018 - 2019

Study (s)

Degree	Center	Acad. year	Period
1402 - Degree in Telecommunications Electronic Engineering	School of Engineering	2	First term

Subject-matter

Degree	Subject-matter	Character
1402 - Degree in Telecommunications Electronic Engineering	12 - Digital electronic systems	Obligatory

Coordination

Name	Department
BATALLER MOMPEAN, MANUEL	242 - Electronic Engineering

SUMMARY

The course ‘Digital Electronic Systems I’ (Sistemas Electrónicos Digitales I) is the first of several courses related to digital electronic systems. The main objective for this course is the study of the basic techniques for the analysis and design of digital systems, setting up the basic knowledge and easing the study of complex systems to be covered in further courses.

This is a compulsory course taught in the third year of the Telecommunication Electronics Engineering degree during the first semester (autumn semester). This course has a length of 6 ECTS from which 3 ECTS are for theory classes, 1 ECTS for problem solving classes and 2 ECTS for laboratory sessions.

This course covers a global vision of digital systems inside the field of digital electronic systems. The proposed topics will allow the student to design a basic digital system and also analysing the requirements needed for implementing a digital design. In order to achieve these goals, the students will learn about different digital systems such as combinational and sequential subsystems, timing circuits, basic digital integrated circuits, programmable logic circuits, etc.

This is a practical course. The principles of digital design are accompanied with examples. Students will perform frequent exercises, both for analysis and design of digital systems which will further test and create in the laboratory.

As a summary, this course provides a basic foundation for design and analysis of digital electronic systems and their associated circuits.

PREVIOUS KNOWLEDGE

Relationship to other subjects of the same degree

There are no specified enrollment restrictions with other subjects of the curriculum.

Other requirements

In order to get the most out of the course, the student must have some previous knowledge and skills obtained in previous courses related to basic electronics. The main requirements are:

Measurement of electronic magnitudes as voltage and current
Use of electronic circuit simulators.
Being used to work in an electronics laboratory: usage of basic equipment, etc.
Logic families: bipolar and CMOS logic.

OUTCOMES

1402 - Degree in Telecommunications Electronic Engineering

- G3 - Acquisition of the knowledge of the basic and technological subjects that allows students to learn new methods and theories and endows them with the versatility to adapt to new situations.
- G4 - Ability to solve problems with initiative, decision-making and creativity, and to communicate and transmit knowledge, abilities and skills, understanding the ethical and professional responsibility of the activity of a telecommunications technical engineer.
- Capacidad de análisis y diseño de circuitos combinacionales y secuenciales, síncronos y asíncronos, y de utilización de microprocesadores y circuitos integrados.
- R10 - Understand and apply the fundamentals of hardware description languages describing hardware devices.

LEARNING OUTCOMES

The learning outcomes in the course Digital Electronic Systems are:

1. Ability to design and analyse combinational and sequential circuits, synchronous and asynchronous (R9)

2. Ability to design and analyse digital circuits using standard SSI and MSI circuits (R9)

3. Ability to design digital electronic systems (G3,G4)

4. Apply digital technologies to solve problems and develop solutions based on digital circuits in different fields of application (G3,G4)

5. Adequate planning and conception of the global structure in a digital system and the relations among all different parts of the design (G3,G4,R9)

6. Efficient use of software tools for design and programming of a digital system, allowing the successful design of the system (G3,G4,R9)

7. Selection of digital integrated circuits, including programmable logic devices (G3)

8. Describe a digital function using a Hardware Description Language (R10)

9. Program a digital device and simulate it by means of a Hardware Description Language (R10)

DESCRIPTION OF CONTENTS

1. INTRODUCTION TO DIGITAL ELECTRONIC SYSTEMS

Systems: Analysis and Synthesis. Boolean algebra. Simplification of logic functions. Logic Families

2. LOGIC SIMULATOR

Multisim: introduction, libraries, simulation types. Simulation of digital systems with Pspice: digital stimuli.

3. COMBINATIONAL CIRCUITS

Definition. Analysis and synthesis. Implementation with NAND and NOR gates. XOR and XNOR functions. Multilevel circuits: hazards.

4. INTRODUCTION TO THE HARDWARE DESCRIPTION LANGUAGES

Historical review. Basics. Data Types. Sequential and concurrent instruction. Subprograms. Test benches.

5. MSI CIRCUITS

Encoders and decoders. Code converters. Multiplexers and Demultiplexers. Comparator circuits. Arithmetic circuits. Arithmetic-Logic Units. VHDL description: decoders, multiplexers and arithmetic circuits. Exercises.

6. FLIP-FLOPS CIRCUITS.

RS flip-flop: synchronous and asynchronous operation. JK flip-flop. Master-slave flip-flop. Flip-flop D. Flip-flop T. VHDL description of the Flip-flops. Exercises.

7. INTRODUCCIÓN A LOS CIRCUITOS SECUENCIALES

Definition. Shift registers. Asynchronous counters. Synchronous counters: introduction and design. Types of counters: up-down, ring, Johnson. Examples of circuits MSI. VHDL description of the counters. Exercises.

8. DIGITAL CIRCUITS AND CLOCK TIMING

Schmitt Trigger gates. Timer circuits with logic gates. Digital timer circuits. Clock circuits with logic gates. Digital astable circuits.

9. UNITED MACHINE DESIGN

Introduction: Moore and Mealy machines. Analysis of synchronous sequential circuits. Synthesis methodology. VHDL description of Moore machine. Introduction to asynchronous sequential circuits. Exercises

10. INTRODUCCIÓN A LA LÓGICA PROGRAMABLE

Tipos de SPLD: PROM, PAL, PLA, GAL. Flujo de diseño. Especificación de tiempos. Introducción a los CPLDs: dispositivos de Altera. Introducción a las FPGAs: familias de Xilinx.

WORKLOAD

ACTIVITY	Hours	% To be attended
Theory classes	30,00	100
Laboratory practices	20,00	100
Classroom practices	10,00	100
Development of group work	10,00	0
Study and independent work	30,00	0
Readings supplementary material	5,00	0
Preparing lectures	20,00	0
Preparation of practical classes and problem	5,00	0
Resolution of case studies	20,00	0
TOTAL	**150,00**	

TEACHING METHODOLOGY

The course is organised around three kinds of attending classes: theory class, problem solving class and laboratory class. Office hours are used as additional attending tool for students. Concerning out-of-classroom activities, additional exercises must be solved, as well as report preparation.

In theory and problem-solving classes, traditional teaching method will be used. In theory sessions the teacher will explain the basic contents of the course using different teaching tools as slide presentation, together with other tools (G3,G4,R9,R10). Problem-solving classes will use two different models. First, the teacher will propose and solve different problems which are essential for proper understanding of digital systems from students, learning to follow a procedure and identify the required elements needed to adequately solve a problem (G3,G4,R9,R10). Second, the teacher will propose a problem and the students must solve the problem being distributed into groups, individually, or using other group working techniques and always under direct supervision of the teacher (G4,R9); once completed, the solutions will be collected by the teacher and corrected by the teacher or the students (depending on the case).

Students have a specific office-hour calendar where the teacher is available in his office for any concern related to the course (problem solving, theory doubts, report guidance, etc.). The attending hours will be detailed at the beginning of the academic year. Additionally, there exist a distance ‘office-hours’ program where questions can be solved using e-mail contact, and it is also promoted the use of the students’ portal ‘Aula Virtual’ provided by the University of Valencia, where all the information related to the course is available online.

Laboratory sessions are organized according to three basic principles: design, mounting (real or virtual mounting) and testing/simulating an electronic digital system (G4,R9,R10). The estimated duration for each laboratory session is 3 hours. The session will be carried out by groups of, at most, two persons. The student will get the laboratory activities’ guide in advance so that previous preparation time is allowed. Once in the laboratory, there exists a direct supervision from the teacher. The student must assume the responsibility for all the stages in the proposal: design, mounting and testing. The final goal of the laboratory is to obtain a working system according to initial specifications. Finally, a lab report will be

required from the teacher (G3,G4,R9,R10).

All of the described activities will be always using the support of 'Aula Virtual' as the most important source of information and communication for the student.

EVALUATION

Assessment of student learning will take place following two models:

a) By assessing the result of the continuous evaluation from the exams (theory, test and laboratory) plus the note of laboratory practices. To qualify for this type of evaluation, the student must have regularly attended classes and theoretical problems. To average the test scores of theory and laboratory will require each of them to equal or exceed 4 The final grade is obtained from the following considerations.

- The theory mark will emerge as a result of carrying on the dates indicated in the official calendar of the written examination. It will consist of five questions of theoretical and practical problems and two (G3,G4,R9,R10). All questions will be related to the contents of the agenda, and with similar issues and problems done in class difficulty. This classification corresponds to 35% of the final grade.
- Upon completion of the course, a multiple-choice test that will count for 20% of the final grade will be made (G3,G4,R9,R10).
- The laboratory note arise as a result of the realization of an individual at the end of the semester, which will include a number of issues directly related to the practices during the course exam (G3,G4,R9,R10). It will consist of the design, assembly and / or simulation of some of the sections made by students throughout the laboratory sessions to which they had to attend. Demonstrated skill, proficiency in the use of laboratory equipment and design development throughout the session will be assessed. To be submitted to the above discussion, is a prerequisite to regularly attended practices (you can not miss more than 1 session). This note is equal to 25% of the final grade.
- In addition to this paper, the performance of the practice site was assessed using a few simple questions at the end of each session (G3,G4,R9,R10). This ongoing evaluation of the work done by students in all lab sessions valued skill, interest and results. This paper translates into 20% of the final grade for the course.
- The final grade for the course will come from the following expression:

- Final Score = 0,35*Ex_Theory+0,25 * Ex_Lab+0,2*Eval_Lab + 0,2 * Ex_Test

b) From a second call in which the qualification of the theory and / or laboratory part can be improved by conducting a test. The exam will be held on the official date and will consist of a theoretical first part, in which the student must demonstrate his knowledge of the concepts and relations seen in class and a second part that will consist of a laboratory examination (G3,G4,R9,R10). In this, the students must complete the design, assembly and / or simulation of specified digital systems related to the contents of the agenda and with similar issues and practices developed in the laboratory scripts difficulty (G3,G4,R9,R10). To average the test scores of theory and laboratory will require each of them to equal or exceed 4. The final grade for the course will leave the following expression:

- Final Score = 0,55*Ex_Theory+0,25 * Ex_Lab+0,2*Eval_Lab

Students who opt for option a), and who do not approve the subject in this way, may submit to the official examination in second call (modality b).

In any case, the evaluation system will be governed by what is established in the Evaluation and Qualification Regulations of the Universitat de València for Degrees and Masters

(https://webges.uv.es/uvTaeWeb/MuestraInformacionEdictoPublicoFrontAction.do?accion=inicio&idEdictoSeleccionado=5639).

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Basic

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Additional

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