COURSE DATA

Data Subject	
Code	34655
Name	Fundamentals of Computers
Cycle	Grade
ECTS Credits	6.0
Academic year	2020 - 2021

Study (s)

Degree	Center	Acad. year	Period
1400 - Degree in Computer Engineering	School of Engineering	1	Second term

Subject-matter

Degree	Subject-matter	Character
1400 - Degree in Computer Engineering	5 - Information technology	Basic Training

Coordination

Name	Department
RUIZ GONZALBO, AURELIO	240 - Computer Science

SUMMARY

The subject "Fundamentals on Computers" is a compulsory on first course in the Degree on Computer Engineering. Set to a commitment of 6 ECTS taught in the second semester of the first course.

The aim of the course is to acquaint students with the fundamentals of computers, primarily from its architecture and programming. We introduce the classical model of von Neumann's computer and using machine language assembler.

The first block introduces the language of computers, machine language, and the student ends up dominating the types of instructions and addressing modes, to continue the instruction formats and the repertoire or set of instructions available. Following the definitions in generic form is passed to particularize the study to a particular processor such as ARMv8. Following the program, then it is intended that the pupil knows the VHDL as a language for describing vehicular hardware. Formal language is introduced and consolidated the various styles of architecture.

Then the goal becomes understanding how the basic building blocks of computer components and their role in the development of architecture. From this point the student will be able to design the data path followed and in turn drive the design of wired and microprogrammed control, both as unicycle and multicycle processors, respectively. Following the same line, then is to get to know one of the main components in the structure of a computer, such as the Arithmetic-Logic Unit (ALU). You learn to design small circuits that are able to perform simple operations such as addition and displacement, and integrated modules capable of complex operations such as multiplication. These modules are the building blocks of the ALU and the main objective is that students learn to design and modify a small ALU able to function properly. The software on the ALU will teach the student integer and floating point arithmetics.

Finally it explores the use of simple programmable devices, inherent to working with HDL and CAD tools, allowing the achievement of ultimate goal: that students become familiar with its use to create small sequential systems using tools that automate repetitive processes for a large number of functions.

PREVIOUS KNOWLEDGE

Relationship to other subjects of the same degree

There are no specified enrollment restrictions with other subjects of the curriculum.

Other requirements

No previous knowledge needed, but this subject is the logic follow-up of Computer Technology, which is taught on the 1st term. Therefore, the students should have studied previously Computer Technology.

OUTCOMES

1400 - Degree in Computer Engineering

- G8 - Knowledge of basic subject areas and technologies that serve as a basis for learning and developing new methods and technologies, and of those which provide versatility to adapt to new situations.
- G9 - Ability to solve problems with initiative, decision making, autonomy and creativity. Ability to communicate and transmit the knowledge, skills and abilities of a computer engineer.
- B3 - Ability to understand and master the basics of discrete mathematics, logic, algorithms and computational complexity and their application for solving problems in engineering.
- B5 - Knowledge of the structure, organisation, operation and interconnection of computer systems, programming fundamentals, and their application for solving problems in engineering.

- B1 - Ability to solve the mathematical problems that may arise in engineering. Ability to apply knowledge of linear algebra, differential and integral calculus, numerical methods, numerical algorithms, statistics and optimisation.

LEARNING OUTCOMES

This course allows for the following learning outcomes:

• Understand how the basic building blocks of computer components and their role in the development of architecture.
• Design simple digital circuits using the fundamental building blocks (gates, FF, registers, counters, PLA).
• Design simple digital circuits using a language of high-level description.
• Work together to make designs and configurations necessary, distributing the workload to deal with complex problems.
• Understand the organization of the SISD architecture and its main functional units.
• Understand how an instruction is executed in a classic machine with a control unit.
• Design the instructions are represented at the level of machine code and in the context of a symbolic assembler.
• Compare and evaluate alternative implementations of the data path and control of a CPU.
• Compare and evaluate alternative implementations of the UAL of a CPU.
• Write simple programs in assembly language.
• Translate key high-level constructs in assembly language and machine.
• Using subroutines in assembler.

To complement the above results, this subject also to acquire the following skills and social skills:

• Capacity for analysis and synthesis
• Ability to argue from rational and logical criteria.
• Ability to communicate properly and organized.
• Ability to personal work.
• Ability to work in groups.

DESCRIPTION OF CONTENTS

1. Sequential circuits

State machines (Mealy and Moore): Performance, construction and description.
Design of a complex digital system.

2. Hardware Description Language (VHDL) and programmable devices

Sintactic elements.
Comportamental, estructural and data flow description.
VHDL description of state machines.
Programming technologies
Programmable Logic Devices: CPLDs, FPGAs.

3. Machine Language

Type of instructions
Format of instructions
Addressing Modes
Particular case: ARMv8

4. Data path. Pipeline

Unicycle processor and control
Pipeline processor and control
Pipeline hazards

5. Arithmetic-Logic Unit

Arithmetic with integers
- Adders/Substractors
- Multiplyers
- Divisors

Floating point Arithmetic
- Format IEEE-754

WORKLOAD

ACTIVITY	Hours	% To be attended
Theory classes	30,00	100
Laboratory practices	20,00	100
Classroom practices	10,00	100
Development of group work	5,00	0
Development of individual work	20,00	0
Study and independent work	5,00	0
Readings supplementary material	5,00	0
Preparation of evaluation activities	20,00	0
Preparing lectures	15,00	0
Preparation of practical classes and problem	15,00	0
Resolution of case studies	3,00	0
Resolution of online questionnaires	2,00	0
TOTAL	**150,00**	

TEACHING METHODOLOGY

The methodology used in the course is based on the conduct of lectures and problems that will be complemented by the student's independent work. The target ratio for each of these activities is as follows:

• theoretical activity.
Description: The lectures will develop the issues by providing a global and inclusive vision, analyzing in detail the key issues and more complex, encouraging at all times, participation of students.
Workload for students on the total load of matter: 19%

• Practical activities.
Description: Complementing theoretical activities in order to apply the basics and expand the knowledge and experience to be acquired in the course of the work proposed. They include the following types of classroom activities:

- classes of problems and issues in the classroom
- discussion sessions and problem-solving exercises and previously worked by the students.
- Practices in Labs
- tutorials scheduled (individualized or group).
- Making of individual evaluation questionnaires.

Workload for students on the total charge of the matter: 21%

• Individual student work.
Description: Realization (outside the classroom) of monographs, literature search directed, issues and problems as well as the preparation of classes and exams (study). This is done individually and tries to promote self- work.
Workload for students on the total charge of the matter: 45%

• Work in small groups.
Description: Realization, by small groups of students (2-4) of work, issues, problems outside the classroom. This work complements the work and encourages individual ability to integrate into working groups.
Workload for students on the total charge of the matter: 15%

It will be used the platform of e-learning (virtual classroom) of the University of Valencia in support of communication with students. Through it you will have access to course materials used in class as well as solve problems and exercises.

EVALUATION

The course evaluation will be performed in the first call preferably by continuous assessment (C) and the evaluation of laboratory activities (L).

The continuous assessment mark (C) is calculated as the average of 3 continuous assessment tests, done during the course, at the end of each group of subjects: P1, P2 and P3. It will de uses the following expression, which reflects the relative weight of each topic:

$$C = 0.35 * P1 + 0.5 * P2 + 0.15 * P3$$

The continuous assessment mark (C) can be improved until 1 point with extra activities (Aext) done during the course, whenever C is greater than or equal to 5, calculating the final continuous assessment mark (Cfin) as:

$$Cfin = C + Aext$$

If continuous assessment mark (C) is greater than or equal to 5 the student may not make the official the first call examination, calculating the note of the first call (N1a) as:

$$N1a = 0.75 * Cfin + 0.25 * L$$

Where laboratory note (L) is calculated as the arithmetic mean of the laboratory session evaluation (SL) and the laboratory test (ExL):

$$L = 0.5 * SL + 0.5 * ExL$$

In the case that the continuous assessment is less than 5, the student should make the official first call examination (Ex1), calculating the note of the first call (N1b) as:

$$N1b = 0.6 * Ex1 + 0.25 * L + 0.15 * C$$

If a student who has passed the first call with continuous assessment (C> = 5) wants to improve his or her note (N1a), He or She may take the examination Ex1, calculating the note 1st call with N1b formula. This will involve refusing the mark given by the formula N1a.

The mark of the second call (N2) is calculated in only one way, from the second call exam (Ex2), the lab notes (L) and continuous assessment (C) defined before. If the lab notes (L) is less than 5, the student will have the option to repeat the laboratory test (EXL).

$$N2 = 0.6 * Ex2 + 0.25 * L + 0.15 * C$$

In any case, the evaluation of this subject will be done in compliance with the University Regulations in this regard, approved by the Governing Council on 30th May 2017 (ACGUV 108/2017)

REFERENCES

Basic

- Patterson/Hennessy. Computer organization and design. ARM Edition. Ed. Elsevier. 2017
- S. Barrachina, M. Castillo, J.M. Claver, J.C. Fernández. Prácticas de introducción a la arquitectura de computadores con el simulador SPIM, Ed. Pearson, 2013
- W. Stallings. Organización y Estructura de Computadores. Diseño para optimizar prestaciones. Ed. Prentice Hall, 2006.
- John Wakerly. Diseño digital. Principios y prácticas 3ª Edición. Editorial Prentice-Hall, 2001.

Additional

- Fernando Pardo y J. Antonio Boluda VHDL Lenguaje para síntesis y modelado de circuitos. Editorial RA-MA, 1999
- S. Brown and Z. Vranesic. Fundamentals of Digital Logic with VHDL Design. 3e. Editorial Mcgraw-Hill Series in Electrical and Computer Engineering), 2005.

ADDENDUM COVID-19

This addendum will only be activated if the health situation requires so and with the prior agreement of the Governing Council

The teaching methodology for this subject will follow the model approved by the Academic Committee of the GII / GIM degrees (https://links.uv.es/catinfmult/modeloDocent). If the facilities are closed because of COVID-19 pandemics, the scheduled lectures will be replaced by synchronous online sessions within the assigned time slots of the course, using the tools provided by the university.

If the facilities need to be closed due to the pandemics causing any of the evaluation exercises to be held at ETSE-UV, these exercises will be substituted by equivalent exercieses held online using the tools provided by the university. The weights for each activity will remain the same as specified in the teaching guide.