

**Developments for the Data Acquisition and  
Control Systems of the ATLAS Tile  
Calorimeter for the HL-LHC**



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Antonio Cervelló Duato

SUPERVISORS

Dr. Jose Alberto Valero Biot  
Dr. José Gabriel Torres Pais

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## Declaration

This dissertation is the result of my own work, except where explicit reference is made to the work of others. It has not been submitted for another qualification to this or any other university.

Antonio Cervelló Duato



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Ah, i a l'arròs al forn.

# Preface

The Large Hadron Collider (LHC) at CERN is the most powerful particle accelerator in the world, enabling physicists to explore the fundamental structure of matter through high-energy proton-proton collisions. Since its commissioning in 2010, it has been at the forefront of particle physics research, facilitating landmark discoveries such as the Higgs boson. Over 7,000 scientists from more than 60 countries contribute to its scientific program, underscoring its role as a truly global research infrastructure. In the coming years, the LHC will undergo a substantial upgrade, known as the High-Luminosity LHC (HL-LHC), which will increase the instantaneous luminosity and deliver up to 7.5 times the integrated luminosity compared to the original design.

The upgrade to HL-LHC imposes new challenges on the LHC experiments, particularly ATLAS. Higher luminosity implies not only an increased number of collisions per bunch crossing, but also more stringent demands on the radiation tolerance, data throughput, and timing synchronization of the detector readout systems. As a result, a complete redesign of the Trigger and Data Acquisition (TDAQ) architecture is necessary. The ATLAS Phase-II Upgrade addresses these requirements by introducing new front-end and back-end electronics, new communication protocols, and an upgraded control and monitoring infrastructure.

This thesis focuses on the development of readout and control systems for the Tile Calorimeter (TileCal), the hadronic calorimeter of the ATLAS de-

tector. In the HL-LHC era, the TileCal readout system is being completely redesigned. This includes new on-detector electronics, a high-speed optical data transmission chain, and a new off-detector readout system based on the Tile PreProcessor (TilePPr). In addition, developments for a dedicated embedded controller, the Tile Computer-on-Module (TileCoM), are introduced for configuration, control, and monitoring.

Chapter 1 and Chapter 2 provide an overview of the LHC and the ATLAS experiment, including the Tile Calorimeter architecture and the motivation for its upgrade. These chapters also detail the performance goals for the HL-LHC and the implications for the ATLAS Phase-II Upgrade, which includes increased detector granularity, improved time resolution, and a higher data acquisition rate.

Chapter 3 describes the developments in the TDAQ software for TileCal. This includes the integration of new tools such as the Software ReadOut Driver (SWROD) and the FELIX devices with high-bandwidth PCIe cards and optical links, enabling flexible and scalable data acquisition as well as other debugging tools.

Chapter 4 details the design and development of tools for the Tile Computer-on-Module (TileCoM), an embedded control system. TileCoM is responsible for the configuration and remote management of the back-end readout electronics, including firmware programming, IPbus communication, and data streaming to monitoring systems via the OPC UA protocol.

Chapter 5 focuses on the hardware development of a custom ATCA Switch Board designed for networking and infrastructure support in the TileCal readout system. The switch board is designed with signal integrity in mind, and verification tests including *iperf3* bandwidth analysis confirmed the correct functionality of all channels.

Chapter 6 presents the setup and results of several testbeam campaigns conducted at CERN's SPS North Area. During these campaigns, prototypes of the upgraded TileCal electronics were tested under beam conditions.

Chapter 7 focuses on the implementation and integration of the Demonstrator project within the ATLAS experiment. It covers the setup and configuration of the FELIX readout system, integration with TDAQ, and tests performed in both the Tile standalone and ATLAS partition. Lastly, it discusses the outcomes of these tests, including calibration data.

Finally, the conclusions summarize the contributions of this thesis to the Tile Calorimeter upgrade effort including future work.

## Personal contributions

The author has contributed to the installation and maintenance of the FELIX and SWROD systems for the Tile Calorimeter, including the design and implementation of multiple plugins and applications for both the main and integrator readout chains.

He has also been actively involved in the firmware and software development for the TileCoM, providing a working AlmaLinux image tailored for the system, enabling communication with an OPC UA server running on the device, and designing the necessary pipelines to automate the system's build and deployment processes.

Additionally, the author led the development of a custom ATCA switch board, from schematic design and PCB layout to the validation and performance testing of the final prototype.

He participated in several testbeam campaigns, contributing to the commissioning of the FELIX and SWROD systems, and supporting all phases of the test campaigns including setup, maintenance, and data-taking operations of the TileCal readout system.

Beyond development and testing for this thesis, the author has played an active role in the operation of the ATLAS Tile Calorimeter, serving as Run Coordinator during the initial phase of Run 3 following Long Shutdown 2 (LS2). In this capacity, he directed daily detector operations and coordinated

the activities of the TileCal operations team. He has also served on multiple occasions as the on-call expert for the TileCal data acquisition system, ensuring reliable performance during data-taking periods. Furthermore, he contributed to the development and maintenance of software components, adding new functionalities and resolving bugs to support the stability and evolution of the TileCal readout infrastructure.

To finalize, the author of this thesis has also contributed through poster and oral presentations at international conferences, peer-reviewed journal publications, and conference proceedings. These contributions are listed below:

### Talks

- Antonio Cervelló. *The TileCal PreProcessor Interface with the ATLAS Global Data Acquisition System at the HL-LHC*, oral presentation at the 15th Pisa Meeting on Advanced Detectors, La Biodola - Isola D'Elba, Italy, 22–28 May 2022.
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- Antonio Cervelló. *Testbeam setup of the ATLAS Tile Calorimeter with Phase II Upgrade Readout Electronics*, oral presentation at the 13th Beam Telescopes and Test Beams Workshop (BTTB2025), Valencia, Spain, 27 May 2025.

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- Antonio Cervelló. *Developments for the ATLAS Tile Calorimeter Read-out System for HL-LHC*, poster presentation at the 2023 IEEE Nuclear Science Symposium (NSS), Medical Imaging Conference (MIC), and RTSD Conference, Vancouver, Canada, 4–11 November 2023.

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# Chapter 1

## CERN and the Large Hadron Collider

*In this chapter, an overview of CERN is provided, with a particular focus on the LHC and the ATLAS experiment. Special attention is given to the Tile Calorimeter subdetector and the current systems associated with it. This background sets the stage for the discussions and analyses presented in this thesis.*

### 1.1 CERN

The European Organization for Nuclear Research (Conseil Européen pour la Recherche Nucléaire) (CERN), stands as the preeminent hub for fundamental research in particle physics. Established in 1954, CERN is located on the Franco-Swiss border near Geneva, Switzerland.

CERN's primary mission revolves around probing the fundamental constituents of matter and the forces governing their interactions. To achieve this, CERN operates a vast array of particle accelerators and detectors, facilitating cutting-edge experiments and discoveries at the forefront of particle

physics.

Beyond its scientific pursuits, CERN fosters international collaboration, welcoming researchers from around the globe to participate in its experiments and projects. This spirit of collaboration and knowledge-sharing has propelled CERN to the forefront of scientific research, cementing its status as a beacon of discovery and innovation in the field of particle physics.

Central to CERN's endeavors is the Large Hadron Collider (LHC) [1], the world's most powerful particle accelerator, renowned for its ability to accelerate beams of protons to unprecedented energies and collide them at near-light speeds. These collisions enable scientists to explore the fundamental properties of matter and delve into the mysteries of the universe.

## 1.2 The Large Hadron Collider

The LHC is hailed as the forefront of particle acceleration technology, earning recognition as the world's largest and most powerful particle accelerator. Located in a circular tunnel 27 kilometers in circumference and reaching depths of up to 100 meters underground, it extends across the border between France and Switzerland.

At its core, the LHC uses the power of superconducting magnets meticulously engineered to guide proton beams into head-on collisions, achieving a staggering center-of-mass energy of  $\sqrt{s} = 13.6$  TeV. This collision energy is complemented by an instantaneous luminosity of  $\mathcal{L} = 1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ , facilitating unprecedented experimental conditions.

The journey towards these collision energies begins far earlier in CERN's accelerator complex (Figure 1.1), a network of interconnected accelerators [2]. Initiating the process, the Linear Accelerator 4 (Linac4) and Proton Synchrotron Booster (PSB) serve as the inaugural stages, propelling the proton beam to an energy of 1.4 GeV. Subsequently, the Proton Synchrotron (PS) assumes control, elevating the beam's energy to 25 GeV. The baton is then

passed to the Super Proton Synchrotron (SPS), where protons undergo further acceleration, reaching energies of 450 GeV, before ultimately being injected into the LHC.

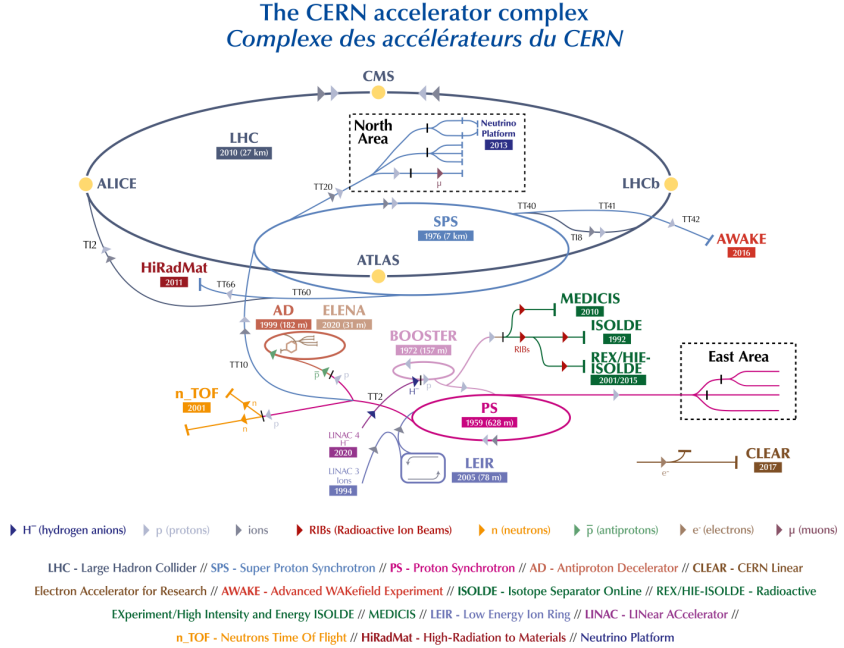


Figure 1.1: CERN accelerator complex.

### 1.2.1 LHC Experiments

Nine experiments at the LHC are used to detect and analyze the several of particles produced by collisions in the accelerator.

The largest experiments at the LHC, namely A Toroidal LHC ApparatuS (ATLAS) [3] and Compact Muon Solenoid (CMS) [4], employ general-purpose detectors to explore a broad spectrum of physics phenomena. The presence of two independently designed detectors is crucial for corroborating any new discoveries. On the other hand, A Large Ion Collider Experiment (ALICE) [5] and LHC beauty (LHCb) [6] feature specialized detectors

tailored to investigate specific phenomena. These four detectors are housed underground in expansive caverns along the LHC ring.

The two largest experiments at the LHC, ATLAS and CMS, are multi-purpose detectors situated on opposite sides of the LHC ring. Both ATLAS and CMS were designed and optimized to precisely measure the properties of the strong and electroweak forces at the TeV scale and to explore potential new physics beyond the Standard Model. In 2012, these experiments jointly announced the discovery of the Higgs boson [7], with a mass of approximately 125 GeV. Meanwhile, the LHCb experiment focuses on B-physics and CP violation, and the ALICE experiment studies quark-gluon plasma through heavy ion collisions.

In contrast, the smallest experiments on the LHC, TOTal, Elastic and diffractive cross-section Measurement (TOTEM) [8] and LHC forward (LHCf) [9], concentrate on "forward particles" – protons or heavy ions that graze past each other rather than colliding head-on during beam collisions. TOTEM utilizes detectors positioned on both sides of the CMS interaction point, while LHCf comprises two detectors situated along the LHC beamline, each positioned 140 meters from the ATLAS collision point.

Monopole and Exotics Detector at the LHC - MoEDAL Apparatus for Penetrating Particles (MoEDAL-MAPP) [9] deploys detectors near LHCb to search for a hypothetical particle known as the magnetic monopole. Meanwhile, Forward Search Experiment (FASER) [10] and Scattering and Neutrino Detector at the LHC (SND@LHC) [11], the two newest LHC experiments, are strategically located near the ATLAS collision point to explore light new particles and study neutrinos.

## 1.3 The ATLAS experiment

The ATLAS experiment [3] serves as one of the two general-purpose detectors at the LHC designed to study the products of p-p collisions at the LHC,



engaging in a broad spectrum of physics inquiries ranging from the Higgs boson to exploring extra dimensions and potential constituents of dark matter. While sharing similar scientific objectives with the CMS experiment, ATLAS employs distinct technical solutions and a unique magnet-system design. Weighing in at 7000 tonnes and spanning 46 meters in length, with a height and width of 25 meters each, the ATLAS detector stands as the largest volume particle detector ever constructed.

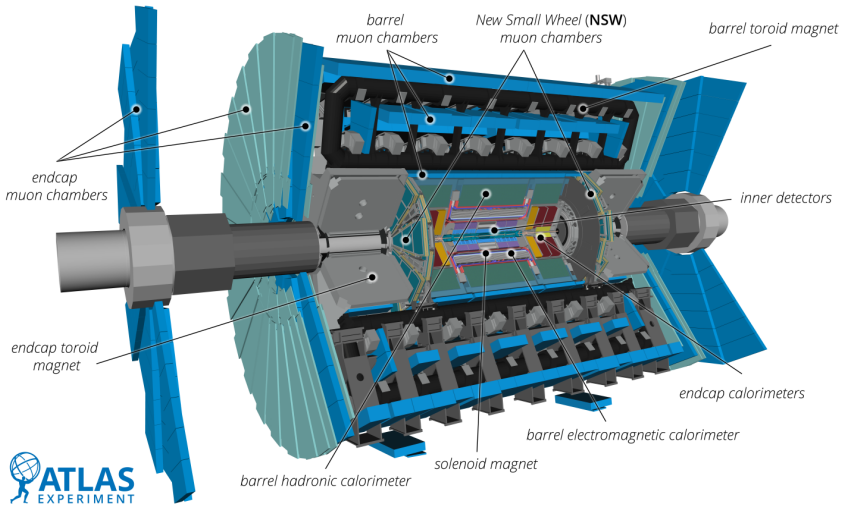


Figure 1.2: The ATLAS experiment.

At the heart of ATLAS, particles from the LHC collide, generating collision debris in the form of new particles that disperse in all directions from the collision point. Six distinct detecting subsystems, arranged in layers around the collision point, record the paths, momentum, and energy of these particles, facilitating their individual identification. A substantial magnet system within ATLAS bends the paths of charged particles, enabling precise measurement of their momenta.

The interactions within the ATLAS detector produce a vast influx of data. To manage this amount of data, ATLAS employs a sophisticated trigger system to discern which events to record and which to disregard. Subsequently, the

data-acquisition and computing systems analyze the recorded collision events.

The Inner Detector (ID) of ATLAS is positioned around the beam pipe, designed specifically for tracking and vertexing by tracing the trajectories of charged particles produced in collisions. Encircling the ID is a solenoidal magnet generating a magnetic field of 2 Tesla, which bends the trajectories of charged particles. This curvature is utilized to calculate the particle momentum.

Surrounding the ID, the Liquid Argon (LAr) calorimeter, which serves as the electromagnetic calorimeter, and the Tile Calorimeter (TileCal), functioning as the hadronic calorimeter, work together to measure the energy deposited by particles and reconstruct their directions. The outermost layer of ATLAS comprises the Muon Spectrometer (MS) and a toroid magnet, where a muon tracking system traces muon trajectories beyond the calorimeters. Three superconducting air-core toroid magnets surrounding the ATLAS detector produce an average magnetic field of 0.5 Tesla, bending the trajectories of charged particles.

The ATLAS detector delivers highly precise measurements of various particle types and processes. Its design requirements encompass several key aspects:

- Excellent electromagnetic calorimetry for distinguishing electrons and photons, complemented by comprehensive hadronic calorimetry for accurate jet and missing transverse energy ( $E_T^{miss}$ ) measurements.
- High-precision muon measurements, ensuring accuracy even at the highest luminosity using the external muon spectrometer alone.
- Efficient tracking at high luminosity to measure high- $p_T$  lepton momenta, identify electrons, photons,  $\tau$ -leptons, and heavy-flavour particles, and reconstruct full events at low luminosity.
- Effective triggering and measurement of low- $p_T$  particles, achieving high efficiencies for most physics processes of interest at the LHC.

- Large acceptance in pseudorapidity ( $\eta$ ) with almost complete azimuthal angle ( $\phi$ ) coverage. Here, the azimuthal angle is measured around the beam axis, while the pseudorapidity is derived from the polar angle ( $\theta$ ) with respect to the plane perpendicular to the beam line:

$$\eta = -\ln\left(\tan\left(\frac{\theta}{2}\right)\right) \quad (1.1)$$

During the Long Shutdown 2 (LS2) that was performed from 2019 to 2021, the Phase-I upgrade project was carried out. The Phase-I upgrades were implemented to address the increased demands of the Run 3 (2022-2026) data-taking period of the LHC. This upgrade phase, completed before the start of Run 3, included improvements to the detector and trigger systems [12]. Figure 1.3 shows the integrated luminosity for ATLAS and CMS since the start of the LHC.

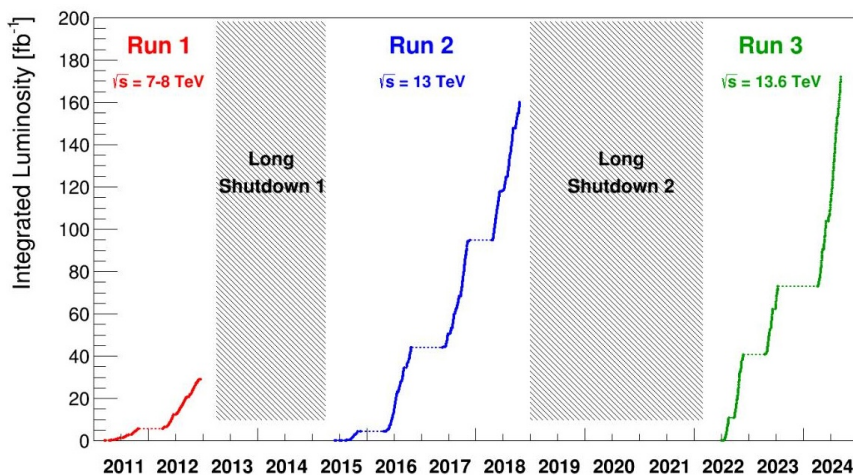


Figure 1.3: Evolution of the integrated luminosity collected by ATLAS and CMS from the start of LHC data taking

Key upgrades in Phase-I focused on enhancing the Level-1 (First-level trigger) (L1) trigger system, including the replacement of the Small Wheel in the muon spectrometer with the New Small Wheel (NSW), based on ad-

vanced detector technologies like MicroMegas and small-strip Thin Gap Chamber (sTGC). The NSW was designed to provide improved tracking and reduce fake muon triggers [13]. The LAr calorimeter also underwent significant improvements with the introduction of a digital trigger system, increasing granularity and energy resolution, enhancing the efficiency of electron and photon triggers [14].

Regarding the Trigger, Timing, and Control (TTC) distribution, the ATLAS Local Trigger Interface (ALTI) module was introduced [15]. The ALTI is a single Versa Module Eurocard (VME) module introduced as a replacement for several legacy modules, including the Local Trigger Processor Interface (LTPI), the Local Trigger Processor (LTP), the TTC VMEbus Interface (TTCvi), and the TTC Emitter (TTCex). The primary role of the ALTI board is to provide an interface between the Level-1 Central Trigger Processor (CTP) and the local TTC system of the sub-detectors.

These upgrades aimed to manage higher event rates while maintaining detector performance and precision. The new systems were commissioned during 2022, with full integration into the ATLAS detector in 2023.

### 1.3.1 Trigger and Data AcQuisition system

The Trigger and Data Acquisition (TDAQ) system [16] has evolved significantly since Run 1 (2010 to 2012) and Run 2 (2015 to 2018) to meet the increasing demands of higher luminosity and data rates at the LHC. Initially designed to handle lower event rates and simpler selection criteria [17], the system has been continuously upgraded with new hardware, software, and algorithms to improve event selection efficiency, precision, and data handling. By Run 3, the TDAQ system incorporated new technologies and configurations (see Figure 1.4) to support more complex physics analyses, taking advantage of improved detector resolution and response times, while maintaining robust performance under higher collision rates [18].

The L1 primarily relies on two independent systems utilizing custom elec-

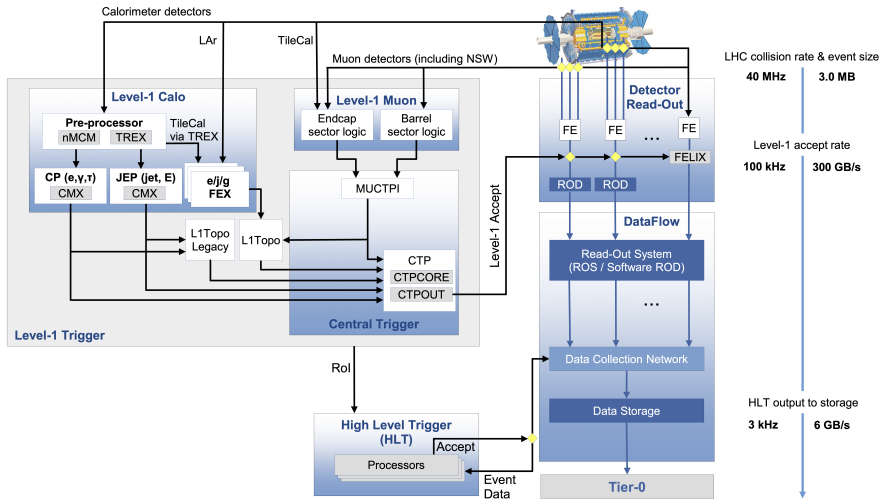


Figure 1.4: The ATLAS TDAQ system in Run 3.

tronics: the Level-1 Calorimeter (L1Calo) and the Level-1 Muon (L1Muon). The Level-1 Topological Processor (L1Topo) system, utilizing kinematic information from reconstructed objects in L1Calo and L1Muon, applies topological selections.

The L1 trigger decision is formulated by the CTP, integrating inputs from the L1Calo, L1Muon, and L1Topo systems, alongside other subsystems such as the Minimum Bias Trigger Scintillators (MBTS), ATLAS Forward Proton (AFP) detector, Absolute Luminosity For ATLAS (ALFA) detector, Luminosity Cherenkov Integrating Detector 2 (LUCID-2) Cherenkov Counter, and Zero Degree Calorimeter (ZDC). The CTP also manages the dead time, which is a mechanism to restrict the number of close-by L1 accepts.

Events satisfying the trigger menu requirements are accepted at rates up to the maximum detector readout rate of 100 kHz, within a fixed latency of below 2.5 microseconds. The CTP can configure up to 512 distinct L1 trigger items.

Accepted events proceed to a software-based High-Level Trigger (HLT). Here, online algorithms reconstruct events with progressively higher levels of

detail, either across the full detector volume or within restricted Regions-of-Interest (RoIs) identified by the L1 trigger. For Run 3, the HLT software framework was redesigned to support multi-threaded execution.

The L1 Trigger reduces the event rate from 40 MHz to 100 kHz, achieving a rejection factor of around 400. The HLT further filters the data using software, achieving an additional rejection factor of about 100 [19].

The Data AcQuisition (DAQ) system itself handles event fragments generated by the detectors, buffering them until a trigger decision is made. It then feeds data to the HLT, constructs complete events, and writes the selected events to permanent storage. Additionally, it provides the necessary control, configuration, and monitoring facilities.

The expected physics output rate of the HLT during ATLAS data-taking runs averages at 3 kHz.

The DAQ system transports data from custom subdetector electronics to offline processing based on trigger decisions. Data compression reduces the original event size of about 3 MB to below 2 MB [18].

## 1.4 The Tile Calorimeter

The TileCal detector [20] within ATLAS is a sampling calorimeter utilizing steel as an absorber and scintillator tiles as the active medium. Positioned behind the liquid argon electromagnetic calorimeter, it covers the region of  $|\eta| < 1.7$ .

TileCal consists of a central Long Barrel, measuring 5.6 meters in length, and two Extended Barrels, each 2.6 meters long. Each barrel is azimuthally divided into 64 wedges of size  $\Delta\phi \sim 0.1$ , made of steel plates and scintillator tiles. With a radial depth of approximately 7.4 interaction lengths ( $\lambda$ ), the entire detector weighs 2,600 metric tons.

The arrangement of scintillator tiles, oriented both radially and normal to the beam axis, in combination with WaveLength Shifting (WLS) fiber readout

along the tile edges, ensures nearly seamless azimuthal calorimeter coverage. These WLS fibers are grouped into bundles defining 5,182 calorimetric cells, which are read out by 9,852 PhotoMultiplier Tube (PMT), providing an approximate projective geometry in pseudorapidity.

The region between the long and extended barrel features specialized cells. Front-end electronics and readout optics are integrated within the mechanical structure of TileCal, with PMTs and all readout electronics housed on aluminum units called super-drawers. These electronics also generate analogue sums of channels with the same  $\eta$  coordinate, forming trigger towers crucial for L1 trigger processing.

For calibration purposes, the calorimeter is equipped with a laser system, a Charge Injection System (CIS), and a  $^{137}\text{Cs}$  radioactive source, ensuring precise calibration of the detector response to the electromagnetic scale. The structure of the TileCal modules is illustrated in Figure 1.5.

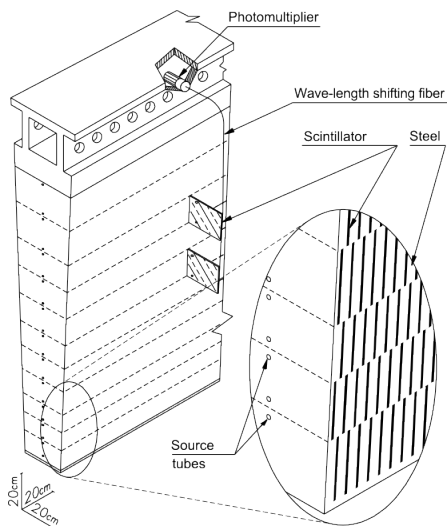


Figure 1.5: Schematic showing how the mechanical assembly and the optical readout of the Tile Calorimeter are integrated together. The various components of the optical readout, namely the tiles, the fibres and the photomultipliers, are shown.

### 1.4.1 Optics

The active medium of TileCal consists of scintillating tiles that come in eleven different sizes [21], each with a thickness of 3 mm. These tiles have radial lengths ranging from 97 mm to 187 mm and azimuthal lengths ranging from 200 mm to 400 mm, with the size of the tiles varying according to their depth within the detector. When ionizing particles pass through the tiles, they generate ultraviolet scintillation light within the polystyrene base material of the tiles. This ultraviolet light is then converted into visible light through WLS fibers.

Each tile is encased in a plastic sleeve that serves two purposes: it protects the tile and enhances the light yield of the scintillation due to its high reflectivity of 95%. The sleeve also contains a mask pattern designed to reduce optical non-uniformity across the tile, achieving a uniformity level below 5% for the combined signals from both sides of the tile. WLS fibers are attached to the edges of the tiles to collect the produced light and shift it to a longer wavelength. These fibers then route the light to the PMTs located within the super-drawers.

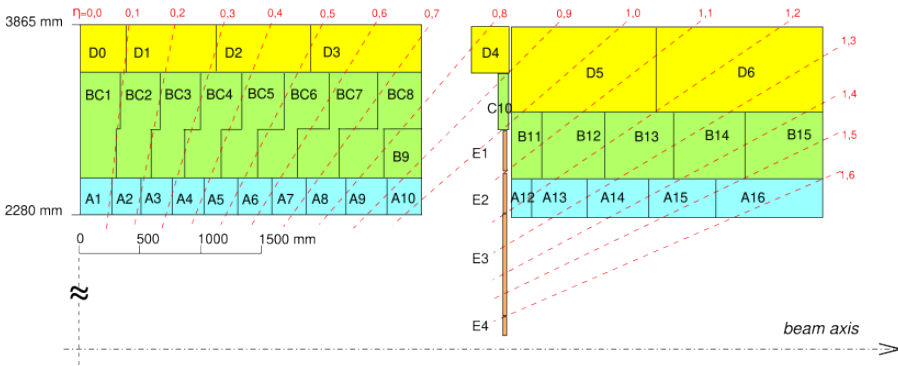


Figure 1.6: Segmentation in depth and in  $\eta$  of the Tile Calorimeter modules in the central (left) and extended (right) barrels. The Tile Calorimeter is symmetric about the interaction point at the origin.



The WLS fibers are grouped into bundles that define a three-dimensional cell structure, creating three radial sampling depths of approximately 1.5, 4.1, and  $1.8 \lambda$  at  $\eta = 0$ . The cells are segmented with dimensions of  $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$  in the first two layers and  $0.2 \times 0.1$  in the last layer. The depth and  $\eta$ -segmentation of both the barrel and extended barrel modules are illustrated in Figure 1.6. Each tile is read out by two different PMTs, providing redundancy and sufficient information to partially equalize signals produced by particles passing through different positions within the calorimeter.

### 1.4.2 Front-end electronics

The Long Barrel and Extended Barrels of TileCal are divided into four readout partitions: Extended Barrel A (EBA), Long Barrel A (LBA), Long Barrel C (LBC), and Extended Barrel C (EBC), as shown in Figure 1.7. Each partition contains 64 super-drawers, resulting in a total of 256 super-drawers across the entire detector.

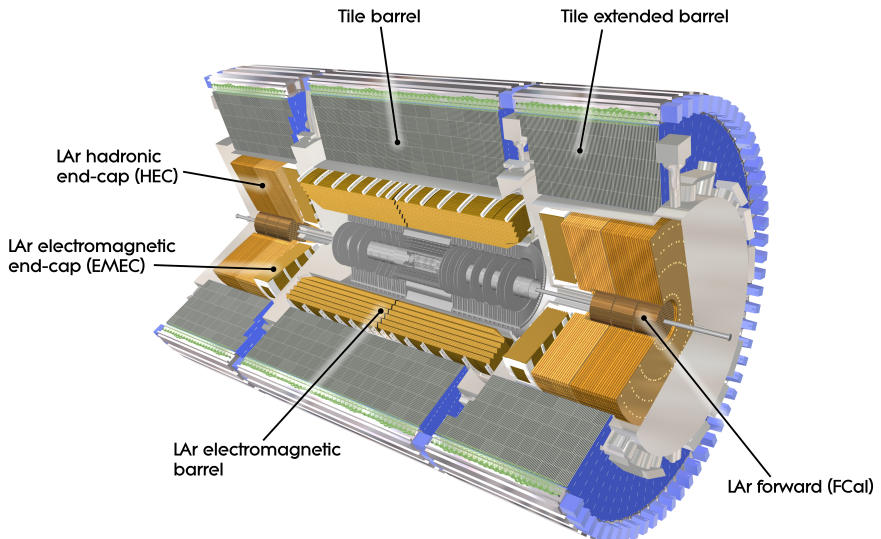


Figure 1.7: A cut-away drawing of the ATLAS inner detector and calorimeters. Tile Calorimeter consists of one barrel and two extended barrel sections and surrounds the LAr barrel electromagnetic and endcap hadronic calorimeters.

The front-end electronics [22] and readout components are housed within these super-drawers, while the remaining trigger and readout electronics are located off-detector. Figure 1.8 provides a block diagram illustrating the TileCal electronics.

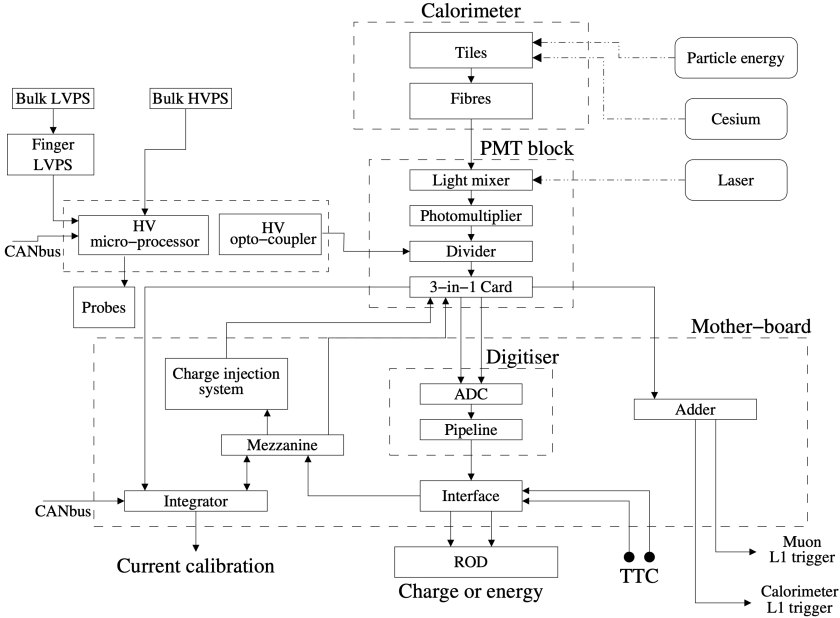


Figure 1.8: Block diagram of the actual TileCal electronics.

### Photomultiplier block

The PMT block is responsible for detecting and measuring the light produced by the scintillating tiles. It consists of a mechanical structure made of a steel cylinder and mu-metal shield for magnetic protection, and contains several key elements: a light mixer, a PMT, a High-Voltage (HV) divider, and a 3-in-1 card (Figure 1.9). The light mixer ensures uniform illumination of the photocathode by mixing the light from the readout fibers. The PMT blocks are precisely inserted into the aluminum structure of the super-drawers, ensuring accurate alignment of the light mixer and the WLS fiber bundle for each tile.

The main components of a PMT block include:

- **Photomultipliers:** The PMT converts light signals from the fiber bundles into electrical charges. The chosen PMT is the Hamamatsu R5900, which has a compact size of  $28 \times 28 \times 28 \text{ mm}^3$  and features a dynode structure with 8 amplification stages.
- **Light mixers:** To eliminate any dependency of the PMT response on the position of the illuminated photocathode surface, a light mixer blends the light from all fibers in the bundle, ensuring no correlation between the fiber position and the illuminated area on the photocathode.
- **Magnetic shielding:** The mu-metal and iron shielding in the PMT block protects against residual magnetic fields from the ATLAS solenoid and toroids, which could otherwise cause variations in gain. This shielding offers protection against magnetic fields up to 500 Gauss in any direction.
- **HV dividers:** These dividers distribute the high voltage among the dynodes of the PMT. The HV divider also acts as a socket, connecting the PMT to the front-end electronics without the need for interconnecting wires, thereby minimizing capacitance and reducing noise and potential connection issues.
- **3-in-1 cards:** These boards provide both high and low gain shaped pulses for the digitizer boards, support the charge injection calibration system, and handle slow integration of PMT signals for monitoring and calibration purposes.

### Digitizer system

The 3-in-1 process the PMT signals by amplifying and shaping them into two output signals, one with high gain and the other with low gain, with a

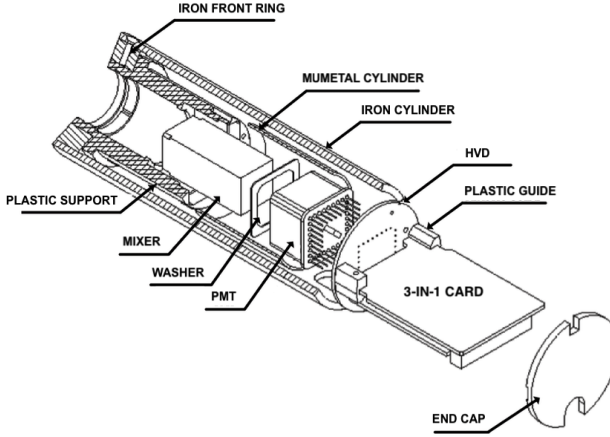


Figure 1.9: Parts and components of a PMT block.

gain ratio of 64. These signals are then transmitted to the Digitizer boards, where they are digitized every 25 ns using 10-bit Analog-to-Digital Converter (ADC). Each Digitizer board contains two depth-configurable pipeline memories, housed in the Tile Data Management Unit (TileDMU) Application-Specific Integrated Circuit (ASIC) [23], that store the digitized data until a Level-1 Accept signal (L1A) is received.

Each TileDMU ASIC handles digitized data from three channels, meaning each Digitizer board manages six channels. When the L1A signal is received, a data frame containing up to 16 samples is copied into derandomizer buffers on the Interface board, preparing it for transmission to the Read Out Driver (ROD) system in the back-end electronics. To reduce total data bandwidth during regular operation, only one of the two gain signals and seven samples are typically read out.

The sampling clock, provided by the TTC receiver (TTCrx) ASIC [24], can be collectively adjusted for all ADCs on a Digitizer board in increments of 106 ps [23]. This phase adjustment ensures that the central sample is near the pulse peak, optimizing signal capture. The motherboard also includes an analog section that supplies a voltage reference to the ADCs and features two

8-bit Digital-to-Analog Converter (DAC)s that provide a pedestal for the AC-coupled inputs.

Each Long Barrel (LB) super-drawer contains up to 8 Digitizer boards, while the Extended Barrel (EB) modules contain 6 Digitizer boards.

### Interface board

The Interface board [25] serves as the digital link between the front-end electronics and the back-end electronics system. Each TileCal module is equipped with one Interface board, which performs several key functions: it receives and distributes TTC signals to the on-board electronics, collects and formats data from the digitizer boards, and transmits the digitized data via an optical link to the ROD system.

The Interface board features a redundant readout system equipped with two output fibers. However, only one of these fibers is actively connected to the ROD system, keeping the other fiber as a backup. Figure 1.10 illustrates a block diagram of the Interface board, detailing its integral components and data flow paths.

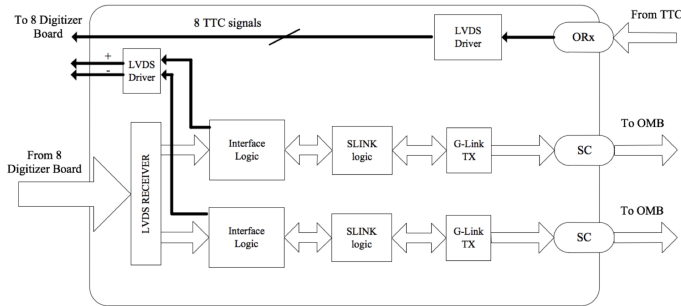


Figure 1.10: Diagram of the data flow and main functional blocks of the Interface board card.

### Adder board

The adder boards play a role in the trigger system by receiving analog signals from up to six 3-in-1 cards that make up a trigger tower. These boards perform

an analog summation of the signals. Two distinct analog sum outputs are generated and sent to the L1 trigger system. The first output is the sum of signals from all cells in the trigger tower, while the second output includes only the signal from the last layer cell. This setup enables precise triggering based on the specific energy deposition patterns in the Tile Calorimeter.

### 1.4.3 Back-end electronics

The back-end electronics system is housed in the counting rooms of the cavern Underground Service Area 15 (ATLAS Counting Room) (USA15), situated 70 meters from the detector where houses essential infrastructure and equipment for the detector's operation [26].

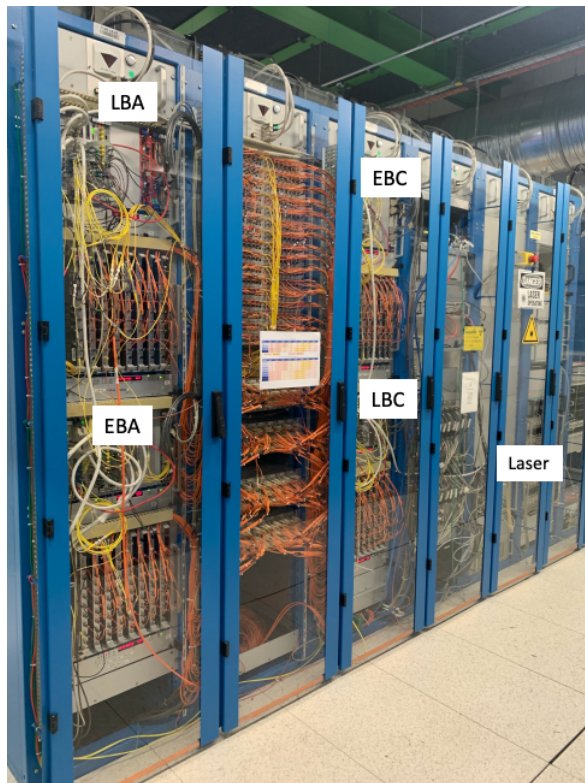


Figure 1.11: Picture of the TileCal back-end electronics racks in USA15.

The back-end electronics comprises two distinct subsystems: the ROD system and the TTC system [27]. The back-end electronics is divided into four partitions, each responsible for the readout of the Long and Extended Barrels. These units are physically separated into different crates: a 6U VME TTC crate and a 9U VME ROD crate, as can be seen in Figure 1.11.

### ReadOut Driver board

The ROD board [28] is a central component of the back-end electronics, responsible for receiving data from eight super-drawers via optical links. To fully read out the Tile Calorimeter, a total of 32 RODs are required, distributed across four VME crates, with eight RODs per crate. Each ROD module (see Figure 1.12 which includes a ROD and four Processing Unit (PU), each equipped with two commercial Digital Signal Processor (DSP) chips that handle data processing before it is sent to the ATLAS DAQ system.

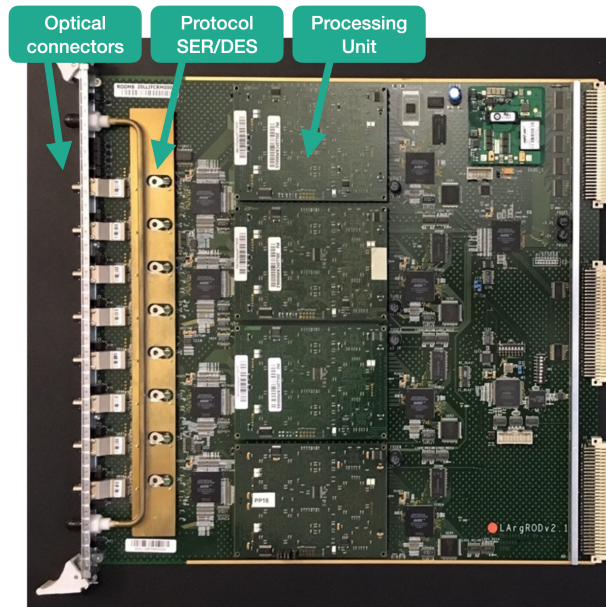


Figure 1.12: Tile Read Out Electronics Board: The optical connector interfaces with the front-end electronics. Each ROD is equipped with four PUs.

Additionally, each ROD crate contains one Trigger and Busy Module (TBM). This 9U VME module manages the distribution of TTC signals from the local TTC system to the RODs and collects busy signals from the eight RODs to generate a combined busy signal for the ROD Busy module. The ROD crate also houses a Single Board Computer (SBC) that is used to configure all the RODs.

### Trigger, Timing and Control

The back-end TTC system is housed in four VME crates, with each TTC partition containing a set of VME boards responsible for managing TTC information across different subsystems.

- **ALTI:** During detector operation, the ALTI module receives TTC signals from the CTP via parallel twisted-pair Low-voltage differential signaling (LVDS) cables, and then distributes these signals to the sub-detector electronics through the optical TTC distribution network. Each complete LHC turn consists of 3564 Bunch Crossing (BC), where a BC corresponds to a discrete time slot in which two proton bunches circulating in opposite directions may collide at one of the detector interaction points [1]. The signals transmitted from the CTP include the bunch clock, orbit signal, L1A signal with an 8-bit trigger type, and the event counter reset. The bunch clock is the primary timing signal generated by the LHC, operating at a frequency of 40 MHz, while the orbit signal marks the start of a new LHC turn and helps identify individual BCs [29].
- **SBC:** This computer is responsible for configuring and controlling all the VME devices connected to the crate.

Additionally, the TTC crate contains other TileCal-specific modules primarily used for calibration, but also involved in handling TTC information:



- **SHared A Few Triggers (SHAFT):** This module controls calibration trigger requests, particularly during physics runs where it shares the calibration request.
- **TTC Receiver in PCIe Mezzanine Card (TTCpr):** The TTCpr module provides TTC information to the TDAQ software during calibration runs. It is installed in the SBC within the TTC crate.
- **Laser Read Out Driver:** This module supplies information from the Laser calibration system to the TDAQ software and distributes TTC signals to the Laser system.
- **TTC Optical Coupler (TTCoc):** Located outside the VME crates, the TTCoc module fans out optical signals to up to 320 different destinations.

The location of the TTC rack was strategically chosen to minimize the length of TTC fibers connecting to the front-end crates, thereby reducing trigger latency. Trigger latency refers to the time difference between the Bunch Crossing Identifier (BCID) and the arrival of the L1A signal at the front-end electronics. Furthermore, the programmable delay lines on the calibration boards are configured to replicate the timing of signals generated by particles originating from the interaction point.

#### 1.4.4 Data flow of the TileCal readout chain

The complete readout process is illustrated in Figure 1.13. It begins with the collection of light produced by particles passing through the TileCal scintillating tiles. This light is then directed to the PMTs via WLS fibers. The PMTs convert the light into an electrical analog pulse, which is subsequently shaped and amplified by the 3-in-1 cards. These cards generate two copies of the analog signal with a gain ratio of 1:64. The analog signals from the PMTs are transmitted to the digitizer boards, where they are digitized at the LHC

frequency and stored in the TileDMUs pipeline memories with configurable depth. Simultaneously, the low-gain analog signals are summed in groups of five and sent to the L1 trigger system.

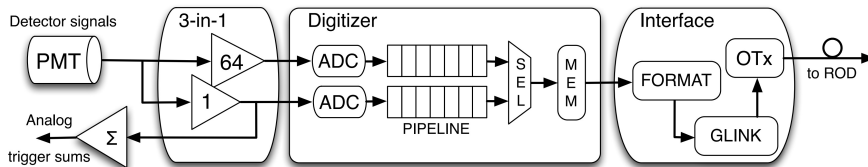


Figure 1.13: Block diagram of TileCal readout chain.

In the L1 trigger system, the CTP sends the L1A signal through the TTC network via the LTP to the front-end electronics, requesting the selected events at an average rate of 100 kHz. Upon receiving the L1A signal, the TileDMU transmits the samples corresponding to the requested BCID to the Interface board. The Interface board then assembles a data fragment containing the samples from all channels in the super-drawer and transmits it to the ROD system in the back-end electronics.

The data flow rate is regulated using a busy feedback signal from the back-end electronics to the CTP. This busy signal is generated by the ROD modules when their input buffers become near full. The signal is transmitted to the TBM and the ROD Busy module, which then relay it to the CTP, indicating that no new events can be accepted until the buffers are cleared.

## Chapter 2

# ATLAS Experiment Upgrades for HL-LHC

*This chapter outlines the upgrades for the HL-LHC system, which will replace the system described in Chapter 1. A detailed explanation of the various improvements introduced during the HL-LHC upgrade is provided, with particular emphasis on the Phase-II upgrade of the Tile Calorimeter.*

The High-Luminosity LHC (HL-LHC) [30] represents a significant upgrade to the existing LHC, aimed at enhancing its capabilities to explore the fundamental aspects of particle physics. Scheduled for completion during the Long Shutdown 3 (LS3) from 2026 to 2030 (see Figure 2.1), the HL-LHC will boost the collider's performance by increasing its nominal instantaneous luminosity to  $\mathcal{L} = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ , which is approximately 7.5 times the LHC original design. This upgrade will significantly increase the number of proton-proton collisions, reaching an average of 200 inelastic interactions per bunch crossing. This will produce high-statistics data essential for precision studies of the Higgs boson and other Standard Model particles, as well as for the search

for new physics such as supersymmetry, dark matter, and long-lived particles. It also enhances sensitivity to rare processes and subtle effects in the flavor sector.

The HL-LHC will deliver an impressive integrated luminosity of 300-350  $fb^{-1}$  annually, with an ambitious goal of reaching 4000  $fb^{-1}$  during its exploitation period. This tenfold increase in integrated luminosity compared to the LHC will enable researchers to explore the properties of the Higgs boson in unprecedented detail. Such advancements are crucial for deepening our understanding of the fundamental forces and particles that constitute our universe.



Figure 2.1: LHC / HL-LHC Schedule Plan [31]. Updated January 2025.

In parallel with the HL-LHC upgrade, the ATLAS detector is undergoing a comprehensive upgrade in preparation for the new operational conditions [32]. This upgrade, known as the ATLAS Phase-II upgrade, is scheduled across three phases corresponding to the LHC's long shutdown periods. The upgrades are essential to handle the increased luminosity and pile-up events (occurrence of multiple proton-proton interactions happening within the same bunch crossing), which will rise from 60 to 200 per beam crossing.

To meet these challenges, the ATLAS detector will see improvements in its

granularity, requiring a new TDAQ architecture capable of managing higher trigger rates and the massive amounts of data generated. Furthermore, the upgrade will necessitate the installation of a new, radiation-tolerant front-end electronics system.

Several sub-detectors within ATLAS, such as the Inner Detector, the LAr Forward Calorimeter, and the Forward Muon Wheels, will need complete replacements due to their vulnerability to radiation damage. However, other components like the calorimeters and muon chambers will only require upgrades to their electronics systems to cope with the new radiation levels and increased data bandwidth. These improvements are necessary to ensuring that ATLAS remains at the forefront of high-energy physics research during the HL-LHC era.

## 2.1 TDAQ Upgrade

The upgraded TDAQ system for Phase-II [33] is designed to handle the complex demands of the HL-LHC era. The system architecture is divided into three primary subsystems: the Level-0 (Trigger System) (L0), DAQ System, and the Event Filter (EF) System, as it can be seen in Figure 2.2.

Data from the ATLAS detectors are fed into the system through three main categories: the Inner Tracker (Inner Tracker (ITk), including pixel and strip detectors), Calorimeters (LAr and TileCal), and the Muon System (Monitoring Drift Tube (MDT), Resistive Plate Chamber (RPC), Thin Gap Chamber (TGC), and NSW). These data are first processed by detector-specific electronics, which are responsible for both readout and initial trigger data preparation.

The L0 Trigger System consists of several components: L0Calo, L0Muon, Global Trigger, and Central Trigger. The L0Calo system is derived from the Phase-I L1Calo system with only minor modifications. It uses coarse-granularity calorimeter data to identify electron, tau lepton, and jet candi-

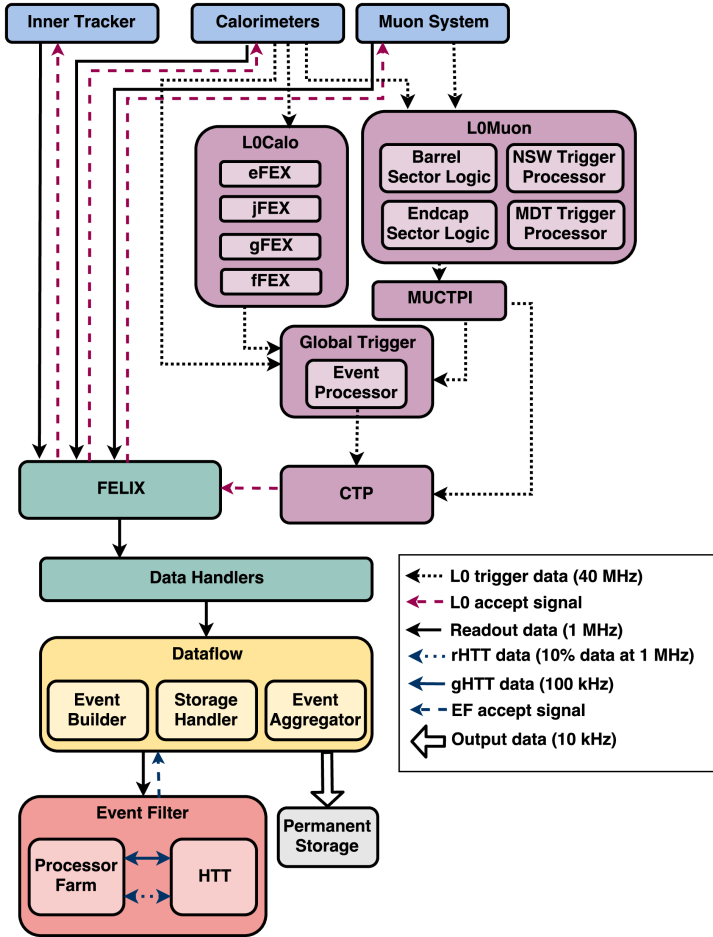


Figure 2.2: Baseline Design of the TDAQ System for Phase-II. The black dotted arrows represent the Level-0 dataflow from the detector systems to the Level-0 trigger components (including Level-0 Calorimeter (L0Calo), Level-0 Muon (L0Muon), Muon-to-Central-Trigger-Processor Interface (MUCTPI), Global Trigger, and CTP) at a rate of 40 MHz. These components must identify physics objects and compute event-level quantities within 10  $\mu$ s. The Level-0 Accept signal (L0A) is sent back to the detectors, as indicated by the red dashed arrows. Trigger and detector data are then transmitted through the DAQ system—comprising Front-End Link eXchange (FELIX), Data Handlers, and the Dataflow subsystem—at a rate of 1 MHz, as depicted by the black solid arrows. For simplicity, direct connections between each L0 trigger component and the Readout system are omitted. The EF system, consisting of a processing farm and a Hardware Tracking for the Trigger (HTT), further reduces the event rate to 10 kHz, with selected events transferred for permanent storage [33].

dates, as well as to calculate missing transverse energy  $E_T^{miss}$ . The L0Muon system processes data from all muon subsystems and the outermost cells of TileCal to identify muons. It also incorporates information from the MDT and RPC to enhance muon trigger coverage. The MUCTPI acts as an interface between the barrel and endcap components of the L0Muon system and the Global Trigger and CTP.

L0Calo and L0Muon utilize calorimeter and muon system information, respectively, to perform an initial event selection at 40 MHz. The Global Trigger refines this selection by applying more sophisticated algorithms, integrating full-granularity data, and calculating complex event-level physics quantities within a 10  $\mu s$  window.

The L0Calo and L0Muon/MUCTPI subsystems send their selected objects to the Global Trigger, including information such as spatial locations, reconstructed energy/momentum values, and discriminant variables. These objects are then combined with the results from the Global Trigger's calorimeter processing to refine selections for electrons/photons, taus, muons, and jets. The CTP forms the final L0A signal, considering the trigger menu configuration, prescale factors, and dead-time requirements, thereby reducing the event rate from 40 MHz to 1 MHz before sending it to the subsequent data acquisition stages.

After the L0 decision, data is passed to the DAQ system, where it undergoes further processing. The DAQ system includes FELIX systems [34], Data Handlers, and the Dataflow subsystem. FELIX serves as a bridge between custom detector links and the DAQ network, while Data Handlers perform detector-specific tasks such as data formatting and monitoring.

The final stage of the process is the EF system, which comprises a large processing farm and a HTT. This system reduces the event rate to 10 kHz, selecting only the most relevant events for permanent storage.

## 2.2 Tile Calorimeter Upgrade

The motivation behind upgrading the Tile Calorimeter [35] is to meet the new demands required for the HL-LHC. The Phase-II Upgrade will involve a complete overhaul of the readout electronics to ensure they can withstand the increased radiation levels and are compatible with the updated TDAQ architecture. This upgrade will allow for more precise and granular data to be provided to the trigger systems.

In the proposed TDAQ architecture, the back-end electronics system will handle the readout of the detector and transmit pre-processed data from cells to the trigger system at the LHCs operational frequency. Simultaneously, data samples will be stored in pipeline memories until a L0A signal is received (see Figure 2.3).

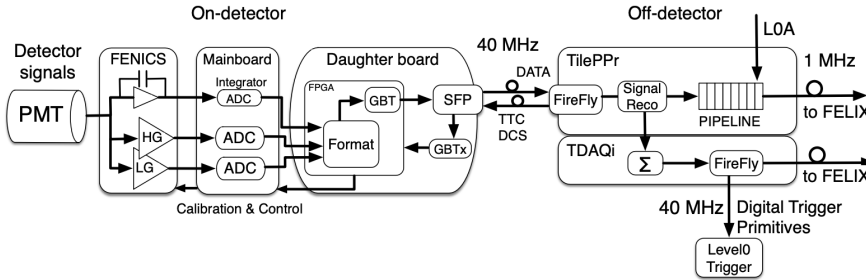


Figure 2.3: Schematic signal and data path for the upgraded Tile Calorimeter: Signal shaping is performed on the front-end board located at the PMT base, digitization occurs on the Mainboard, and high-speed communication is handled by the Daughterboard. The off-detector Tile PreProcessor (TilePPr) processes and streams data to the DAQ system and trigger processors via the Trigger and Data Acquisition interface (TDAQi) module.

To accommodate the new architecture, there will be a significant increase in the bandwidth and number of links between the front-end and back-end electronics systems, along with the use of high-speed links between the back-end electronics and trigger systems (see Table 2.1). The current system utilizes 256 optical links, each with a bandwidth of 800 Mbps. However, the new readout architecture will require 4096 optical links (including redundancy),



each capable of transmitting data at 9.6 Gbps. This substantial upgrade is essential to support the increased data rates and ensure the system's reliability under the challenging conditions of the HL-LHC.

| Downlinks           | Current       | Phase-II  |
|---------------------|---------------|-----------|
| # links             | 256           | 2048      |
| Bandwidth per link  | 80 Mbps (TTC) | 4.8 Gbps  |
| Uplinks             | Current       | Phase-II  |
| # links             | 256           | 4096      |
| # boards            | 32 (VME)      | 32 (ATCA) |
| # crates            | 4 (VME)       | 4 (ATCA)  |
| Bandwidth per link  | 800 Mbps      | 160 Gbps  |
| Bandwidth per board | 6.4 Gbps      | 1.28 Tbps |
| Total Bandwidth     | 165 Gbps      | 40 Tbps   |

Table 2.1: Comparison between the current and Phase-II readout systems.

### 2.2.1 Mechanics

The Tile on-detector electronics and PMTs will be installed in 256 super-drawers (128 long barrel drawers and 128 extended barrel drawers) [35], each three meters long, which slide into the girders of the Tile modules. Each super-drawer is divided into four independent units known as mini-drawers. In addition to housing the on-detector electronics and PMTs, the mini-drawers also provide electrical, optical, and cooling services, offering improved conditions for servicing under future high-radiation environments.

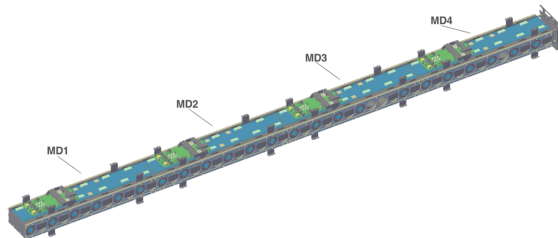


Figure 2.4: Tile super-drawer architecture for a long barrel module.

The updated layout of a Tile super-drawer for a long barrel is illustrated in Figure 2.4. Each mini-drawer can accommodate up to 12 PMTs along with front-end amplifier/shaper cards, a Mainboard, a Daughterboard, and a HVBus board.

The design of the new super-drawer is well-aligned with the cell structure of the long barrel module, which requires up to 45 PMTs, necessitating the use of all four mini-drawers for electronic boards. However, the extended barrel modules require up to 32 PMTs, leaving some mini-drawers without instrumentation. Specifically, mini-drawers MD3 and MD4 house only four and six PMT blocks, respectively. In theory, all 32 PMT blocks in the extended barrel could be read out using only three sets of electronic boards, thereby saving resources compared to the baseline design shared by both the barrel and extended barrel. The super-drawer for a extended barrel module consists of five units: three mini-drawers, each supporting one set of electronic boards, and two smaller units called micro-drawers, each housing two PMT blocks (see Figure 2.5).

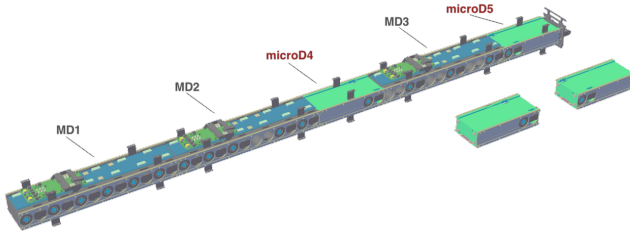


Figure 2.5: Tile super-drawer architecture for a extended barrel module.

### 2.2.2 On-Detector Electronics

The on-detector electronics for the Tile Calorimeter are housed within modular mechanical structures called mini-drawers, as seen in the previous section. The Mainboard receives PMT signals and routes them to the high-speed Daughterboard, which manages communication with the back-end electronics.

Since these electronics are exposed to the high-radiation environment of the HL-LHC, they are designed to be radiation-tolerant, ensuring reliable operation and longevity throughout the detector's lifetime.

### **PMT Block**

The PMT block and its components are illustrated in Figure 2.6. This block includes a light mixer, a PMT, an active HV divider card, and a front-end card that amplifies signals, provides control functions, and enables charge-injection calibration. Additionally, the front-end system integrates and digitizes the current from minimum bias events and from a  $^{137}\text{Cs}$  calibration capsule, which is moved through all Tile cells using a hydraulic tube system. Below is a detailed explanation of the main components:

- **PMT:** Approximately 90% of the PMTs (Hamamatsu R7877) [36] will be reused, with around 10% ( $\sim 1000$ ) new Hamamatsu R11187 PMTs being deployed in the most radiation-exposed regions of the detector due to their enhanced stability.
- **High-Voltage Active Divider (HVAD):** The HVAD is responsible for distributing HV across the PMT dynodes, ensuring a linear response. The current passive HV dividers will be replaced with active dividers, which offer improved response stability at high anode currents.
- **Front-End board for the New Infrastructure with Calibration and Signal Shaping (FENICS) Card:** The FENICS card (Figure 2.7) handles the analog processing of the PMT pulse [37]. It shapes and amplifies the PMT signal, supports calibration, and is used for luminosity measurements. The card provides pulse shaping with two gain settings (x0.4, x16) covering a dynamic range of 0.2 pC to 1000 pC. It also integrates current measurements with five gain settings (0.02 - 13000 nA) for  $^{137}\text{Cs}$  calibration and luminosity studies, and features a built-in Charge Injection System for ADC calibration.

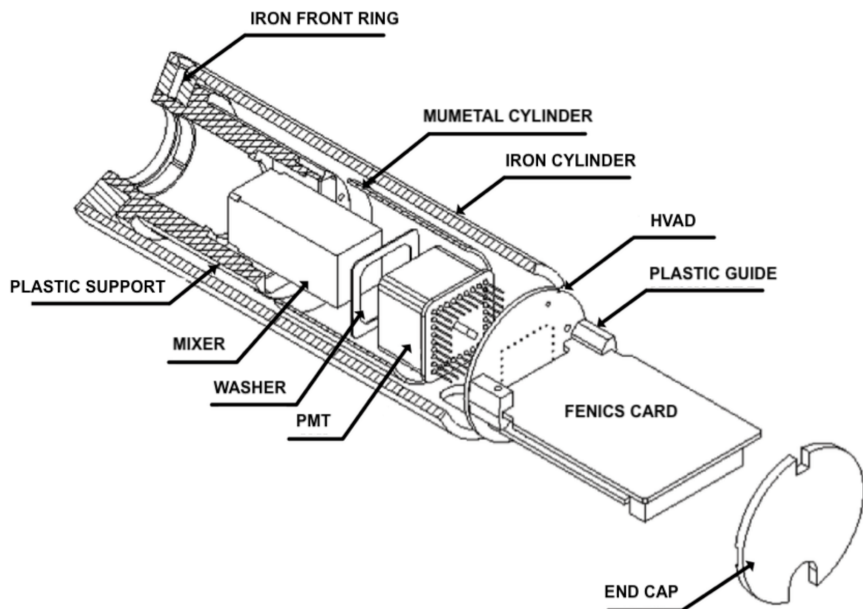


Figure 2.6: Diagram of the PMT block and associated components for Phase-II.

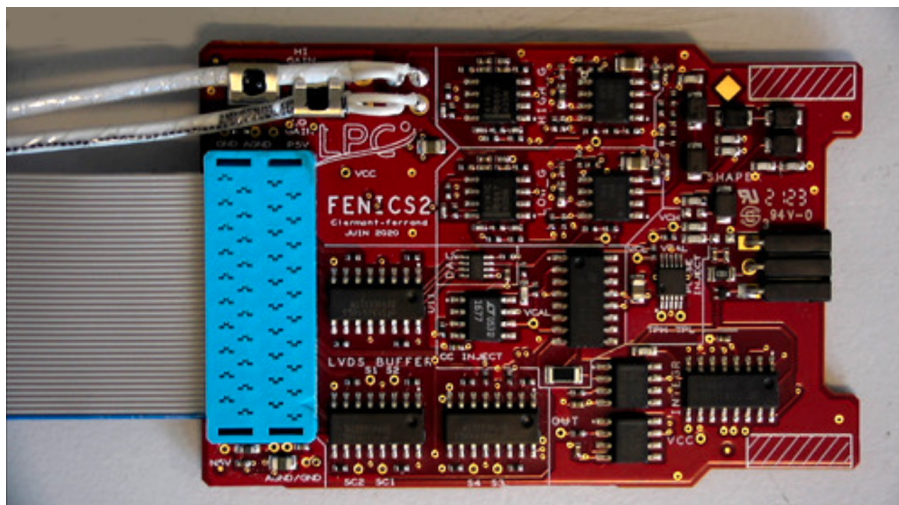


Figure 2.7: FENICS card for signal shaping, amplification, and calibration in the Tile Calorimeter.

## Mainboard

The Mainboard (Figure 2.8) manages signals from up to 12 PMTs and is responsible for key operations such as analog signal routing, signal shaping, amplification and digitization [38]. Some of the key technical features are:

- **Signal Routing and Processing:** The Mainboard receives analog signals from the PMTs, which are first routed through the FENICS card for shaping and amplification. The Mainboard handles both high-gain and low-gain signal paths, providing an effective dynamic range of up to 17 bits for accurate signal capture.
- **Digitization:** The board is equipped with high-speed ADCs that digitize the shaped signals at a sampling rate synchronized to the LHC clock. The ADCs offer a resolution that ensures precise quantization of the analog signals.
- **Field-Programmable Gate Array (FPGA) Integration:** These FPGAs are responsible for managing the timing synchronization of the digitized signals. They adjust the sampling clock phases to compensate for signal propagation delays due to different path lengths from the PMTs, ensuring that the timing information remains consistent across all channels.
- **High-Speed Data Transmission:** The digitized data is transmitted to the off-detector electronics via the Daughterboard, which interfaces directly with the Mainboard.
- **Power Management and Redundancy:** The Mainboard is designed with redundant power supplies to enhance reliability, particularly under the harsh radiation conditions expected in the HL-LHC environment. Each Mainboard is divided into two independent power domains, with each domain powering half of the PMTs. This design ensures that a

failure in one power domain does not compromise the entire board's functionality.

- **Slow-Control Interface:** The Mainboard includes a slow-control interface for monitoring and controlling various operational parameters. This interface allows for real-time diagnostics and adjustments, ensuring optimal performance of the on-detector electronics.
- **Power distribution:** The Mainboard also serves as a power distributor for the Daughterboard.

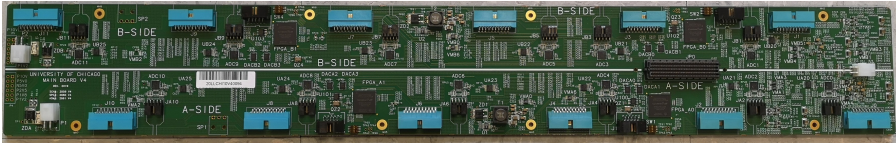


Figure 2.8: Picture of the Mainboard version 4.

## Daughterboard

The Daughterboard (Figure 2.9) is responsible for managing high-speed data transmission and interfacing between the Mainboard and the off-detector systems [39]. Some of the key technical features are:

- **High-Speed Data Transmission:** The Daughterboard is equipped with optical transceivers that support data rates of up to 9.6 Gbps



Figure 2.9: Picture of the Daughterboard version 6.4.

per optical link, enabling the rapid transfer of digitized data to the off-detector electronics. The board typically manages multiple high-speed links, ensuring that large volumes of data generated by the detector can be transmitted without bottlenecks.

- **Data Formatting and Packaging:** Before transmission, the Daughterboard organizes the data into frames suitable for transmission over the optical links, ensuring that the information is correctly formatted for processing by the off-detector electronics.
- **Synchronization and Timing:** The Daughterboard receives timing signals from the TTC system and ensures that the data transmitted to the off-detector systems is accurately synchronized with the LHCs bunch crossing events. This synchronization is essential for accurate event reconstruction and timing alignment across the detector.
- **Error Detection and Correction:** To ensure data integrity during transmission, the Daughterboard includes error detection and correction mechanisms. These mechanisms help to identify and correct errors that may occur during the high-speed transmission of data.
- **Redundant Data Paths:** The Daughterboard is designed with redundancy in mind. It typically includes multiple data paths to ensure that, in the event of a failure in one path, the data can still be transmitted via an alternate route.
- **Power Management:** The Daughterboard is equipped with its own power management systems. The board includes voltage regulators and protection circuits to safeguard against power surges or drops that could affect data transmission.
- **Control Interface:** The Daughterboard includes a control interface that allows it to communicate with the Mainboard and the off-detector electronics. This interface is used for configuration, status monitoring,

and control operations, enabling the Daughterboard to adapt to different operational modes and conditions as required by the TDAQ system.

### 2.2.3 Off-Detector Electronics

The off-detector electronics of the Tile Calorimeter for the HL-LHC upgrade (Figure 2.10) will be comprised of 32 TilePPr modules and 32 TDAQi Rear Transition Module (RTM).

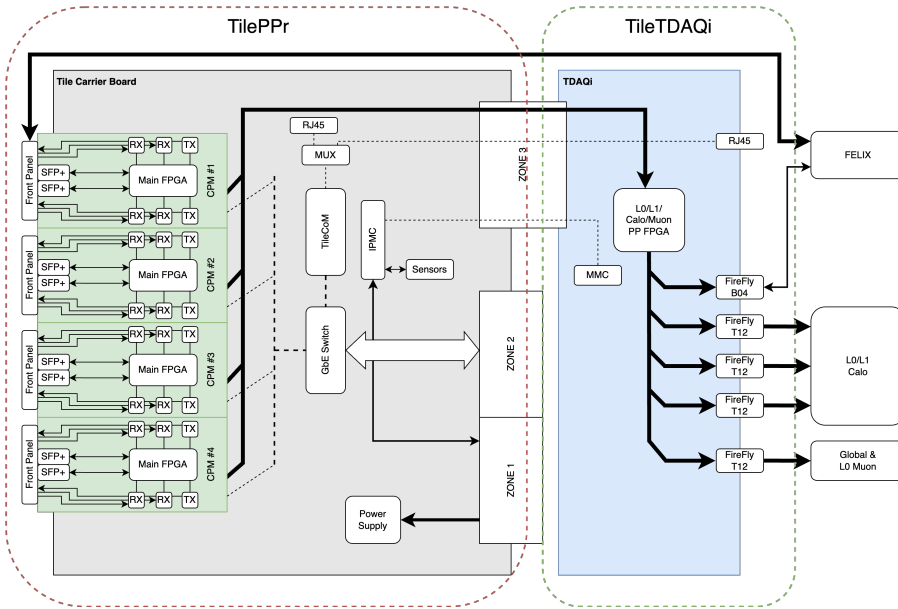


Figure 2.10: Block diagram of the TileCal off-detector electronics. A full TilePPr system is capable of processing data from eight TileCal super-drawers.

#### TilePPr

The TilePPr serves as the interface between the on-detector electronics and the central systems of the ATLAS experiment, including DAQ, Detector Control System (DCS), and the Trigger systems [40]. The TilePPr is designed to handle the high data rates and increased processing demands required by the HL-LHC upgrades. Each TilePPr module is based on an Advanced Telecommunications



Computing Architecture (ATCA) ATCA Carrier BaseBoard (ACBB) that houses four FPGA-based Compact Processing Module (CPM). The ACBB is designed as a cutaway ATCA carrier board that interconnects the CPMs with the TDAQi system via the Zone 3 connector.

**ATCA Carrier BaseBoard** The ACBB is the foundational hardware platform for the TilePPr, designed to house and interconnect various processing modules. It supports up to four full-size Advanced Mezzanine Card (AMC) where the CPM will be inserted, providing the necessary infrastructure for power distribution, clock management, and high-speed communication.



Figure 2.11: ACBB board version 1.2, including the TileCoM, IPMC and GbE switch mezzanine boards.

- **Power Distribution:** The carrier board is responsible for distributing power to each of the CPMs, ensuring stable operation across all modules. It includes redundant power supplies and power monitoring systems

to maintain reliability and fault tolerance, crucial for operation in the HL-LHCs demanding environment.

- **Clock Management:** The ATCA board integrates a centralized clock distribution system that provides precise timing signals to all connected AMCs. This ensures synchronization across the TilePPr, which is essential for the accurate reconstruction of time-critical data from the TileCal detector.
- **High-Speed Communication:** The carrier board includes high-speed backplane connections that enable data transfer between the AMCs and the back-end systems. These connections support multiple protocols, including the GigaBit Transceiver (GBT) protocol for deterministic data transmission, which is critical for meeting the latency requirements of the ATLAS TDAQ system.

**Compact Processing Module** The CPMs are the central processing units and high-speed interfaces of the off-detector electronics for the Tile Calorimeter at the HL-LHC [41]. These modules facilitate high-speed communication between the on-detector electronics and the ATLAS TDAQ system. In total, 128 CPMs distributed across 32 ACBB will be required to manage the readout of the entire Tile Calorimeter during the HL-LHC era.



Figure 2.12: Compact Processing Module version 2 board.

Each CPM is responsible for operating two TileCal modules: one long barrel containing up to 45 PMT channels organized across four mini-drawers, and one extended barrel containing 32 PMT channels distributed across three mini-drawers.

- **High-Speed Interface:** The optical high-speed interface between the on-detector electronics and the CPMs is implemented through four uplinks (operating at 9.6 Gbps) and two downlinks (operating at 4.8 Gbps) per mini-drawer, using the GBT protocol. The uplinks transmit 12-bit digitized PMT signals and monitoring data to the CPMs, while the downlinks provide DCS commands and configuration settings to the on-detector electronics. Additionally, the downlinks deliver the bunch-crossing clock used for sampling the PMT signals.
- **Data Processing and Transmission:** The CPMs are tasked with reconstructing and calibrating the energy deposited in each calorimeter cell in real-time from the digitized detector data. The reconstructed cell energy is then transmitted to the TDAQi module. To meet the timing requirements of the ATLAS trigger system, the data must be processed and transmitted with a maximum latency of  $1.7 \mu\text{s}$  from the collision time to the reception of the computed trigger objects.
- **Data Storage and Trigger Response:** In parallel with the trigger data path, the main FPGA on the CPMs stores the incoming detector data and reconstructed cell energy in Random-Access Memory (RAM)-based pipeline memories until a L0A signal is received. Once this trigger signal is received, the corresponding event data is transmitted to the FELIX system through high-speed links using the FULL Mode protocol, supporting a maximum trigger rate of 1 MHz.
- **Timing and Control:** In the opposite direction, the FELIX system provides the CPMs with TTC information, along with the bunch-crossing

clock, via a GBT link operating at 4.8 Gbps. All high-speed interfaces are designed to operate with fixed and deterministic latency, ensuring the precise timing required for accurate data processing and trigger decision-making in the ATLAS experiment.

**Tile Computer-on-Module** The Tile Computer-on-Module (TileCoM) (Figure 2.13) is a custom designed mezzanine card in a Double Data Rate 4 (DDR4) Small Outline - Dual In-line Memory Module (SO-DIMM) format that plays a role in the configuration, control, and monitoring of both on-detector and off-detector electronics within the TileCal system [42].

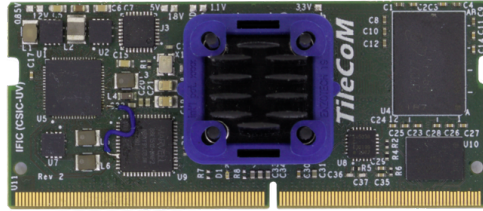


Figure 2.13: TileCoM board version 2.

Some of the key functions of the system are:

- **Remote Configuration and Programming:** The TileCoM is responsible for remotely configuring and programming the FPGAs present in both the on-detector and off-detector electronics. Remote programming is achieved via Transmission Control Protocol/Internet Protocol (TCP/IP), where FPGA configuration files, such as bitstreams, are transmitted from external servers to the TileCoM.
- **Interface with ATLAS TDAQ System:** The TileCoM manages slow control operations, system configuration, and communication for calibration and operational purposes. The TileCoM utilizes the Internet Protocol bus (IPbus) protocol, a flexible Ethernet-based control system, to facilitate the communication between the CPMs and the TileCoM.

- **Integration with DCS:** The TileCoM also interfaces with the ATLAS DCS to acquire and monitor data from approximately 2000 sensors distributed across the TileCal modules. It implements two Open Platform Communications (OPC) servers to manage this data, ensuring real-time monitoring and control. The TileCoM transmits sensor data to the DCS, providing continuous status updates on the health and performance of the TileCal electronics.
- **System-on-Chip (SoC) Design:** The TileCoM is built around a Zynq UltraScale+ ZU2CG SoC, which integrates a dual-core ARM Cortex-R5F-based Real-Time Processing Unit. The integration of the ARM processor within the TileCoM allows for the execution of a Linux operating system. This capability not only facilitates the management of complex tasks such as remote configuration, system monitoring, and real-time data processing but also provides a robust and flexible software environment.

A more comprehensive examination of the firmware and software developments, along with the hardware architecture, can be found in Chapter 4.

**GbE Switch** Figure 2.14 displays the baseline version of the Gigabit Ethernet (GbE) Switch Module, a custom-designed board built around the Broadcom BCM5396 [43], a chip that operates as an unmanaged 16-port GbE switch. In the ACBB, there are three ports dedicated to each AMC bay (a total of 12 ports), one port connected to the TileCoM, one port linked to Zone 3, and two ports interfacing with two channels of the Zone 2.

**Intelligent Platform Management Controller** The Intelligent Platform Management Controller (IPMC) interfaces with the Shelf Manager via the Intelligent Platform Management Bus (IPMB) located in the Zone 1 connector. The IPMC is implemented using a mezzanine card developed at CERN [44],

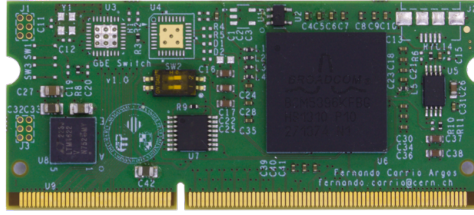


Figure 2.14: GigaBit Ethernet switch board version 1.

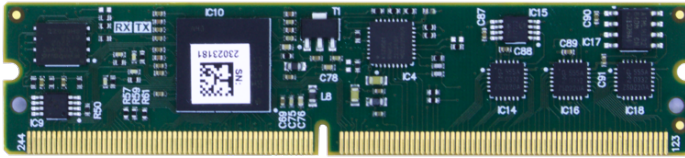


Figure 2.15: IPMC board version 1.

based on the Pigeon Point IPMC and compliant with the ATCA standard Revision 3.0.

The IPMC manages several functions, including hot-swap operations, handling Field Replaceable Unit (FRU) information (such as AMCs and RTMs), and controlling switches, Light Emitting Diode (LED), and hardware addresses. Additionally, it monitors on-board sensors to track temperature, current, and voltage levels, while also detecting events and issuing alarms as necessary. At its core, the IPMC uses a Microsemi A2F200 microcontroller featuring an ARM Cortex M3 processor.

The IPMC connects to the Shelf Manager through redundant Inter-Integrated circuit (I2C) links in the Zone 1 backplane and is powered by a 3.3 V service voltage, which is activated when the ACBB is inserted into an ATCA shelf. It also enables the DC/DC converter to supply the 12 V needed by the AMC cards, RTM, and other payload components within the ACBB.

### Trigger and Data Acquisition interface

The TDAQi serves as the interface between the TilePPr and the TDAQ system [45]. The TDAQi is implemented as an ATCA RTM, ensuring it complies with the ATCA standards. Its primary function is to receive real-time cell energy data from the CPMs connected to the TilePPr. The TDAQi processes these data to generate trigger primitives. These trigger primitives include information about various detector events with different granularity and precision levels, which are then transmitted to the appropriate trigger processors, such as the L0Calo and L0Muon trigger system and various Feature Extractor (FEX) modules.

The TDAQi module is equipped with multiple high-speed optical transceiver modules, which handle the communication between the CPMs, the FELIX system, and the ATLAS trigger processors. An AMD Kintex Ultrascale FPGA is used as the main processing unit in the TDAQi, responsible for implementing the high-speed data links, processing algorithms, and maintaining fixed and deterministic latency across all interfaces. Additionally, the module includes a Module Management Controller (MMC) for power management, sensor monitoring, and communication with the IPMC on the ACBB.

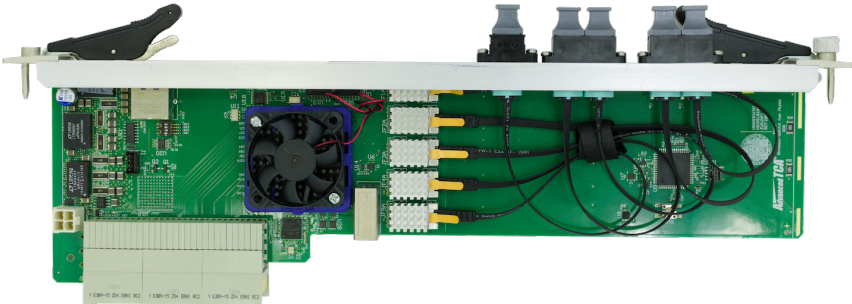


Figure 2.16: TDAQi version 3 board.

### 2.2.4 Power systems

The operation of the upgraded TileCal electronics relies on two independent power distribution systems: the Low-Voltage (LV) system and the HV system. These systems are designed to provide reliable, efficient, and radiation-tolerant power delivery under the challenging conditions of the HL-LHC.

#### Low-Voltage system

The LV system for the TileCal electronics operates in three stages (Figure 2.17). The first stage involves the auxiliary board, which supplies auxiliary power and transmits control signals to the Low-Voltage Power Supply (LVPS) boxes [46].

The second stage involves on-detector LVPS bricks, which convert 200 VDC to 10 VDC, the necessary voltage for powering the on-detector electronics. These LVPS units are based on Commercial Off-The-Shelf (COTS) components. However, due to their placement within a mini-drawer, they are the most radiation-exposed components in TileCal. Extensive irradiation testing identified radiation-hard components suitable for this environment.

To increase the system's robustness, the monitoring and control functions of the LVPS have been separated. Monitoring and control are managed by a radiation-hardened version of the Embedded Local Monitor Board (ELMB). The new ELMB2 board, used for this task, maintains functional equivalence with the legacy ELMB. Control of each low-voltage converter is executed via a passive system implemented on the ELMB-motherboard (ELMB-MB). This system utilizes tri-state voltage levels to reduce cabling requirements, enabling individual control of each Mini-Drawer LVPS. Additionally, each half of the Main Board and Daughter Board is powered by its own power converter, minimizing the impact of any single component failure on the overall system performance. The ELMB-MB also provides power to the ELMB2 board. An LV box is composed of eight LVPS bricks, along with an ELMB and ELMB-MB board, a fuse board, a cold plate, and associated cabling.



The third stage of the LV system consists of point-of-load regulators located directly on the MainBoard and DaughterBoard. These regulators ensure precise power distribution at the component level.

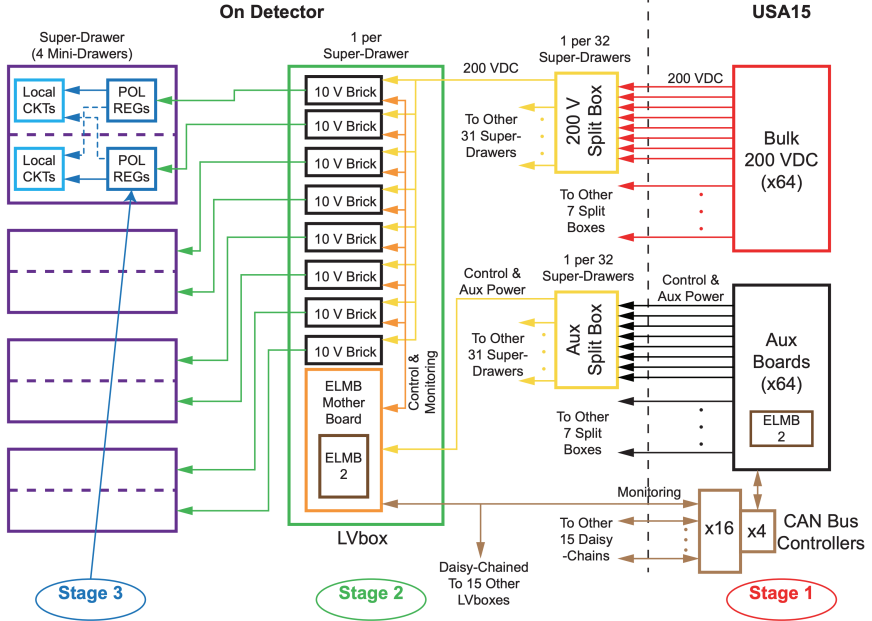


Figure 2.17: Block diagram of the TileCal low-voltage distribution system for the HL-LHC upgrade. The 10V bricks represent the converters that step down 200 VDC to 10 VDC. The third stage of the system is integrated directly onto the front-end electronics boards.

### High-Voltage system

The HV upgraded (Figure 2.18) system consists of HV-remote boards and HV-supply boards, which are located away from the detector in specially designed HV crates [47]. These crates house the HV-remote boards and HV-supply boards, connected to the on-detector components via approximately 100-meter-long HV cables.

Inside the detector, passive HVBus boards distribute the high voltage individually to each PMT located within the mini-drawers. The HVRemote

boards regulate the HV for each PMT through a dedicated regulation loop, which is an adapted version of the loop used in the current legacy system. This adaptation allows for a simplified design since the boards are now positioned off-detector, away from radiation exposure. The regulation loop ensures that the high voltage is maintained within a precision of 0.5 V.

The system requires 256 HVRemote boards to operate, and a significant improvement in the upgraded system compared to the legacy system is the addition of ON/OFF control for each group of four channels, along with individual jumpers for each channel. A single HV input, either -830 V or -950 V, is provided for every 24 channels, with each channel's voltage being individually regulated over a range of approximately 360 V.

The only on-detector components of the HV distribution system are the HVBus boards, which are fully passive and feature four layers to protect the HV tracks within the inner layers of the board.

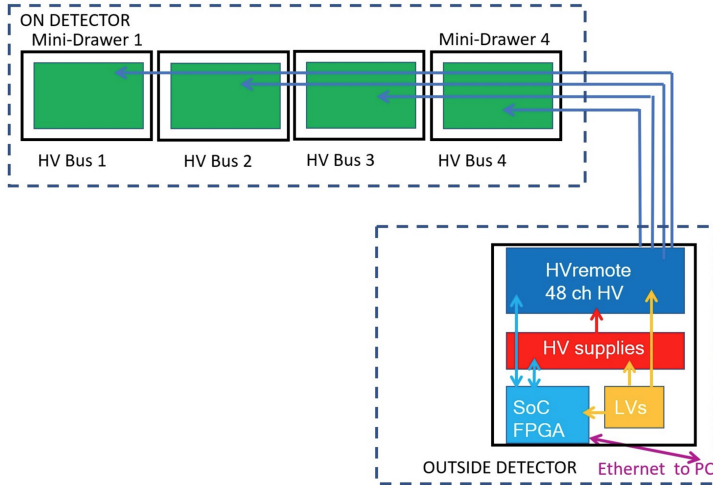


Figure 2.18: HV power supply system layout for the Phase-II upgrade. The regulation system is located remotely, away from the detector, with HV delivered to the detector modules via numerous 100-meter-long cables. Inside the detector, the HV is distributed to 4 mini-drawers in the Long Barrel modules and 3 mini-drawers in the Extended Barrel modules.

### 2.2.5 Calibration systems

To achieve precise calibration of the Tile Calorimeter and accurately measure the individual components of the detector's readout chain, a set of calibration systems is employed, as illustrated in Figure 2.19 [48]. The reconstructed energy of each PMT for a given event,  $E(\text{GeV})$ , is calculated from the raw signal response,  $A(\text{ADC})$ , using the relationship from Equation 2.1:

$$E(\text{GeV}) = A(\text{ADC}) \times C_{\text{ADC} \rightarrow \mu\text{C}} \times C_{\mu\text{C} \rightarrow \text{GeV}} \times C_{\text{Cesium}} \times C_{\text{Laser}} \quad (2.1)$$

This calibration formula is determined for each channel of the Tile Calorimeter. The calibration factors may change over time due to instabilities in the PMTs response, which can be caused by high light fluxes or the aging of optical components. The calibration systems are designed to monitor these instabilities and provide per-channel calibration. The conversion constant from pC to GeV,  $C_{\mu\text{C} \rightarrow \text{GeV}}$ , was established during dedicated test beam campaigns [49]. The remaining calibration constants are provided by the following systems:

- **CIS** to monitor the electronics and determine the conversion factor from ADC counts to pC.
- **Laser system** to monitor the PMTs and associated electronic components.
- **Movable Cesium gamma-source** to calibrate the optical components and PMT gains.

Additionally, the integrator system, which monitors beam conditions and the Tile Calorimeter optics through minimum bias current measurements, is used in conjunction with Laser and Cesium calibration results to track and understand channel gain deviations. For the Tile Calorimeter Phase-II upgrade, both the laser and Cesium systems will undergo significant updates.

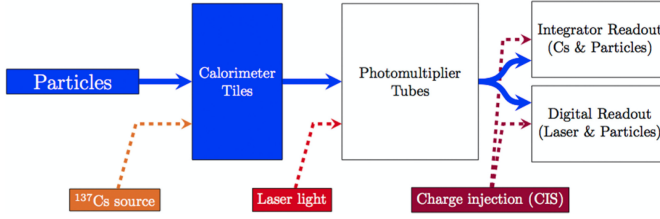


Figure 2.19: Scheme of the Tile Calorimeter calibration chain.

### Interface for the Laser system to the New Acquisition infrastructure

Interface for the LAsER system to the New Acquisition infrastructure (ILANA) [50] is the upgraded interface for the TileCal Laser system, designed to align with the structure of the current laser calibration systems, the Laser Calibration (LASCAR)[51] used during Run 1 and 2. ILANA will be responsible for the following tasks:

- Controlling the laser pump, filter wheel and shutter.
- Injecting a known charge to calibrate the photodiode.
- Measuring the signals from the PMTs and photodiodes.
- Recording the time of arrival of the PMT signals.

ILANA will transmit data to FELIX at a rate of approximately 1 MHz (L0A rate) and will receive TTC and control signals from FELIX.

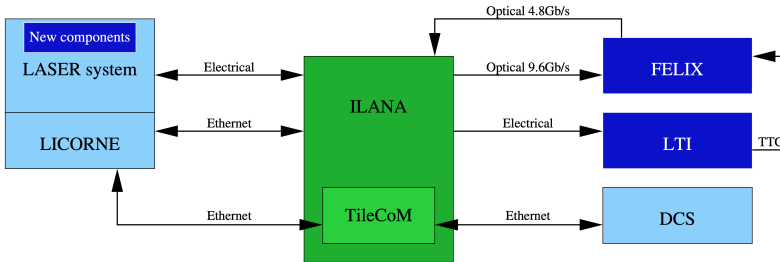


Figure 2.20: Block diagram of the ILANA system.

## Cesium

The Tile Calorimeter's Cesium system will maintain the architectural and mechanical structure of the existing design while introducing enhancements to support increased operational demands [52]. The new system will include 402 Sensor based in INductance (SIN) for capsule detection, 9 Geiger counters for Cesium source detection, and 56 pressure sensors. The system will comprise three independent monitoring setups for the three TileCal barrels, with up to 11 Cesium-boxes on each side of the detector.

New control cards will be introduced, including SIN+Embedded Monitoring and Control Interfaces (EMCI) cards for capsule detection, Garage+EMCI cards for lock control, and ADC cards for pressure measurements. A key improvement is the adoption of optical data transfer, enhancing communication efficiency and data integrity. Additionally, the Cesium system will be fully integrated into the TileCal DCS, allowing comprehensive monitoring and control via EMCI linked to Embedded Monitoring Processor (EMP). These upgrades ensure that the Cesium system will maintain precise calibration and robust performance under the challenging conditions of the HL-LHC.

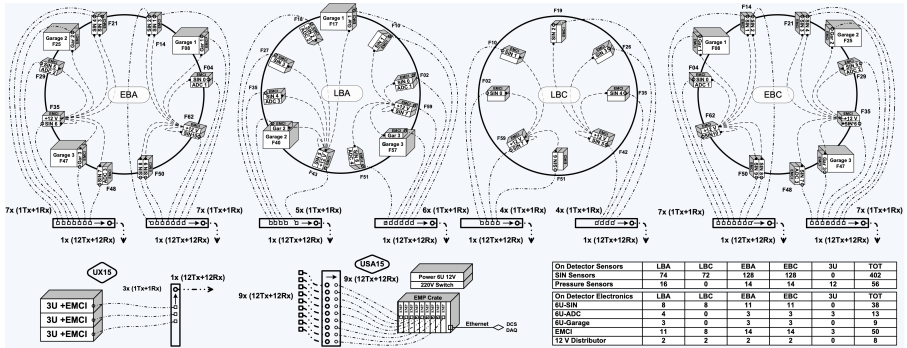


Figure 2.21: The schematics of the control and operation equipment structure of the TileCal Cesium system.



## Chapter 3

# Data Acquisition System developments

*This chapter provides an overview of the developments in the data acquisition system for the ATLAS experiment regarding the Phase-II upgrade presented in Chapter 2, focusing on the TDAQ software and the Tile Calorimeter software. Detailed descriptions of the hardware and software components, their roles, and interactions within the ATLAS detector's data flow are presented.*

### 3.1 TDAQ software

The TDAQ software framework is a highly complex system consisting of around 30,000 applications running on approximately 3,000 Linux nodes in a networked environment [53] [54]. This system must efficiently manage and synchronize a multitude of tasks required to transfer, select, and build events at an average rate of 100 kHz (1 MHz for Phase-II). Additionally, the TDAQ software tracks and responds to both ATLAS and LHC states, ensuring the system remains flexible as configurations change from run to run or even dur-

ing a run (e.g., trigger configurations). Given the complexity, error conditions are not uncommon and advanced recovery mechanisms are implemented to maintain high operational efficiency, achieving 94% during Run 1 and 95.6% during Run 2 [55].

The software is structured around three core subsystems; configuration, control, and monitoring, which work together to maintain seamless operations. The Resource Manager (RM) controls access to system resources, ensuring exclusive or shared usage based on the configuration database. It can limit the number of application instances per partition, host, or globally. The Access Manager (AM) manages user and role-based authorizations for system actions. The Process Manager (PMG) starts and stops processes across the system, relying on RM and AM services for operational feasibility, and runs on each node. Inter-Process Communication (IPC) allows communication between TDAQ applications, while the Remote DataBase (RDB) distributes Object Kernel Support (OKS) configuration across the system. Figure 3.1 shows a simplified overview of the system between different nodes.

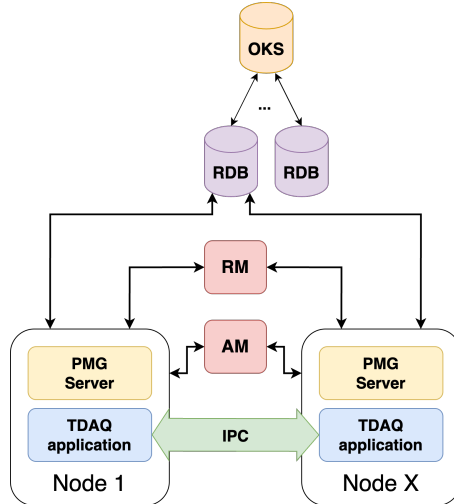


Figure 3.1: Simplified overview of the TDAQ software architecture, highlighting the interaction between the configuration, control, and monitoring subsystems, and their core components.



The Run Control (RC) system converts the configuration of the ATLAS TDAQ into a fully operational data-taking system, ensuring smooth and stable acquisition processes. It is structured as a hierarchical tree of applications, where *Controllers* manage groups of child nodes, with the *RootController* at the top, overseeing the overall system. At the lower levels, *Applications* function as the leaf nodes, representing specific tasks such as ROD applications or HLT tasks, allowing for precise control of each part of the data-taking process.

The online error recovery system in ATLAS has two main components: the local unit and the global unit. The local unit addresses segment-level issues by restarting applications or pausing triggers and reports to the global unit, which handles system-wide errors like clock selection. The system uses stopless removal, which allows data taking to continue by masking malfunctioning components, and stopless recovery, which re-integrates previously disabled components back into the system without interrupting data flow. These mechanisms minimize disruptions and maximize data-taking efficiency [56].

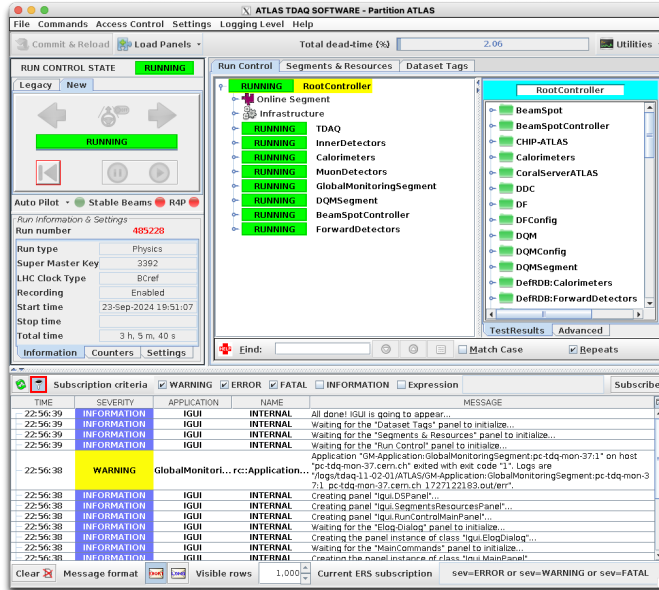


Figure 3.2: The ATLAS TDAQ software Integrated Graphical User Interface (IGUI) panel

Most applications implement a common Finite State Machine (FSM) pattern, ultimately reaching a *RUNNING* state suitable for data-taking operations. The operator interacts with RC via an interface called IGUI (see Figure 3.2). The tasks of the IGUI interface can be broadly categorized into three main functions. First, it monitors the system status by displaying the global state of the TDAQ system and the ATLAS run, while also reporting errors and messages generated by the system. Second, it provides control functionality, allowing interaction with both the TDAQ Run Control and the Online Recovery system. Lastly, it facilitates configuration by enabling the presentation and modification of the TDAQ system settings.

### 3.1.1 The OKS database

The TDAQ system relies on the OKS database to define the content and behavior of any data-taking session, specifying details like which detectors are included and trigger parameters. OKS is an object-oriented database with schema, inheritance, and relationships stored in eXtensible Markup Language (XML) format, which is managed through *git*. The main objects in the database include Partitions, Segments, Applications, Resources, and Computers [57].

A Partition refers to a set of hardware and software resources involved in a data-taking session. ATLAS primary partition is responsible for physics data collection, while other partitions handle subsystem tasks like detector calibrations, such as Tile standalone partition. Each partition contains segments, which are self-sufficient components that can be independently configured and controlled. Segments can represent entire detectors or subsystems, and can also include nested segments, applications, and resources. Applications refer to processes that perform specific tasks and are linked to segments for configuration and control, typically using a FSM model. Resources are the smallest elements within the TDAQ system that can be individually disabled or enabled without disrupting data-taking. These resources can be grouped into

resource sets for collective control, where disabling one element may impact others within the group.

The partition defines which segments and resources are active during a run, while segments represent the building blocks of the system, and they can include other segments or applications. In the configuration database, resources and applications are tied to segments, while resource sets describe interconnected resources that may need to be simultaneously disabled or enabled. A resource set allows linked elements to be managed together, while applications correspond to processes running on designated hosts or computers within the system. Applications can be categorized into several types: infrastructure applications, which provide essential services; run control applications, which synchronize with the system's FSM; and custom lifetime applications, which have defined start and stop points based on system conditions.

The OKS configuration database stores all information about partitions, segments, resources, and applications. Dependencies between applications can also be managed, where one application's startup or shutdown may depend on others. Furthermore, software repositories link applications to specific software versions and external packages, ensuring the system runs compatible processes.

### **3.1.2 Run Control and Finite State Machine**

The RC framework of the TDAQ system operates based on a distributed FSM that ensures synchronized and homogeneous control across multiple applications and hardware components. Each application and controller follows a predefined set of transitions and states, structured hierarchically, enabling consistent operation and communication throughout the entire system.

The RC Framework is a hierarchical, distributed framework where multiple controllers form a tree structure, with a top-level controller (Root Controller) managing transitions for the whole TDAQ system. This structure guarantees synchronization between different system components by ensuring that all controllers must finish the previous transition before moving to the next.

| RC Command    | Source RC State | Target RC State | Description of RC Command                                                                                                      |
|---------------|-----------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------|
| INIT_FSM      | NONE            | NONE            | Starts RC FSM.                                                                                                                 |
| STOP_FSM      | NONE            | NONE            | Stops RC FSM.                                                                                                                  |
| INITIALIZE    | NONE            | INITIAL         | Starts the RootController and calls the necessary PC and SBC for control.                                                      |
| SHUTDOWN      | Any RC State    | NONE            | Terminates the system operation. For normal shutdown, INITIAL is used, but forced termination from any state is also possible. |
| CONFIGURE     | INITIAL         | CONFIGURED      | Acquires configuration parameters from OKS and prepares the system for operation.                                              |
| UNCONFIGURE   | CONFIGURED      | INITIAL         | Disconnects and reverts to INITIAL state.                                                                                      |
| CONNECT       | CONFIGURED      | CONNECTED       | Establishes connections between sub-systems or within submodules.                                                              |
| DISCONNECT    | CONNECTED       | CONFIGURED      | Confirms disconnection between the subsystems.                                                                                 |
| CONFIG        | INITIAL         | CONNECTED       | Automatically runs both CONFIGURE and CONNECT.                                                                                 |
| UNCONFIG      | CONNECTED       | INITIAL         | Automatically runs both DISCONNECT and UNCONFIGURE.                                                                            |
| START         | CONNECTED       | RUNNING         | Starts the system operation and data collection.                                                                               |
| STOPROIB      | RUNNING         | ROIBSTOPPED     | Stops the operation of RoIB.                                                                                                   |
| STOPDC        | ROIBSTOPPED     | DCSTOPPED       | Stops the DCM's operation.                                                                                                     |
| STOPHLT       | DCSTOPPED       | HLTSTOPPED      | Stops the HLT's operation.                                                                                                     |
| STOPRECORDING | HLTSTOPPED      | SFSTOPPED       | Stops data recording.                                                                                                          |
| STOPARCHIVING | SFSTOPPED       | GTHSTOPPED      | Stops data archiving.                                                                                                          |
| STOPGATHERING | GTHSTOPPED      | CONNECTED       | Stops information collection from the detector system.                                                                         |
| STOP          | RUNNING         | CONNECTED       | Runs the series of STOP commands in order until STOPARCHIVING.                                                                 |

Table 3.1: Summary of run control command transitions, including the source and target states [58].

The FSM defines a series of states and transitions that each application or controller can go through (see Figure 3.3 and Table 3.1). The FSM for the TDAQ system is key to ensuring that each segment of the system (hardware controllers, data flow applications, etc.) performs the necessary actions in a coordinated manner. FSM states are categorized based on what each part of the system is doing, whether initializing, connecting, or starting data acquisition [56].

The hierarchical nature of the FSM allows for finer control over specific sub-systems. For instance, while the Root Controller manages the overall system, leaf controllers at the lower levels deal with individual applications (e.g., those controlling hardware components or performing data-taking tasks). The hier-

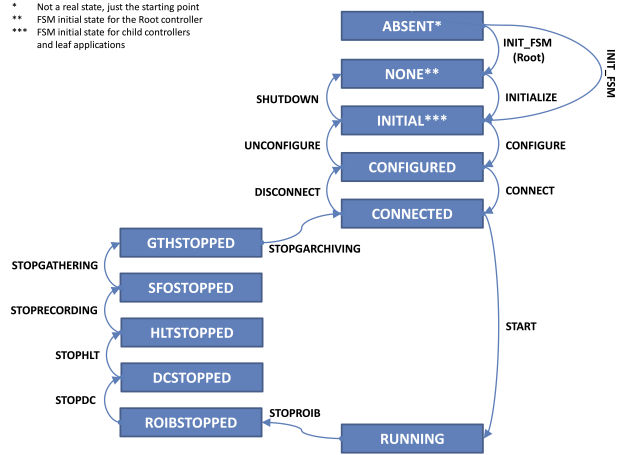


Figure 3.3: Diagram of the ATLAS Run Control Finite State Machine, showing states as blue boxes and labeled transitions connecting them.

archical FSM structure ensures that, once a top-level transition is initiated, all child and leaf controllers move through their respective states, ensuring that no part of the system is out of sync whenever a run is being taken.

A run is a continuous period during which ATLAS collects data. All applications enter a *RUNNING* state in the FSM, and each run is assigned a unique Run Number. When a run ends, for example, when LHC collisions cease, applications exit the *RUNNING* state and triggers are disabled. A new run starts when the system transitions back into the *RUNNING* state with a new Run Number.

### 3.1.3 Tile Calorimeter software

The Tile Calorimeter partition in ATLAS is composed of several segments. One segment is dedicated to monitoring, collecting event data during data-taking to be displayed in the Data Quality Monitoring (DQM) system for real-time verification. Another segment is responsible for minimum bias monitoring, collecting integrator data for luminosity measurements. The Tile Laser system segment controls the LASCAR system. Additionally, there are four seg-

ments corresponding to the readout partitions of the detector, each managing specific detector resources.

Each segment in the Tile Calorimeter partition is associated with specific resources:

- **TTC ROD Crate DAQ (TTCRCD)**: Responsible for configuring the ALTI board, ensuring proper synchronization and timing for each physical partition of the TileCal detector.
- **ROD ROD Crate DAQ (RODRCD)**: Manages the configuration of legacy ROD boards, handling the data acquisition for each partition.
- **TMDB ROD Crate DAQ (TMDBRCD)**: Configures the Tile Muon Digitizer Board (TMDB), which digitize the muon data; enabled only for the Extended Barrel segments.
- **ReadOut System (ROS)**: Merges data from all the RODs of a partition, preparing it for further processing and transmission to the HLT system.
- **ROS Event Builder (REB)**: The REB is responsible for merging data from all ROSeS across different partitions into a single data file. This functionality is specifically available in the Tile Standalone partition, used primarily during calibration runs.
- **TilePPr**: Configures the TilePPr demonstrator, which handles real-time processing of data and manages minimum bias readings. This is specific to the LBA partition, where the demonstrator module (LBA14) is located. A more detailed explanation of the demonstrator module will be given in Chapter 7 .
- **Minimum Bias (MB) system**: Responsible for configuring the minimum bias system, which collects integrator data necessary for luminosity measurements and system calibration.

- **DAQ to DCS communication system (daq2dcs):** Facilitates the communication between the DAQ and the DCS systems.

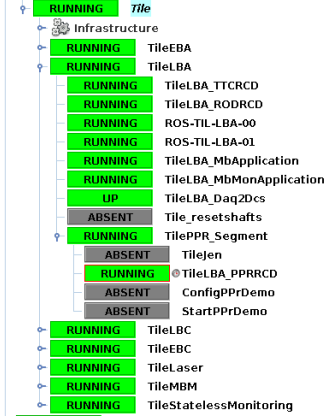


Figure 3.4: View of the active segments in the Tile Calorimeter during data taking in ATLAS.

### 3.1.4 Data packet formats

The ATLAS data packet format consists of several hierarchical components: the Full Fragment, the ReadOut Buffer (ROB) fragment, and the ROD fragment. Additionally, a sub-fragment header—specific to each detector—is included, although this component is implemented outside of the standard ATLAS event format [59].

| Bits                |               | 31                      | 24 | 23            | 16 | 15        | 8 | 7 | 0 |
|---------------------|---------------|-------------------------|----|---------------|----|-----------|---|---|---|
| Sub-Fragment Header | Header Marker | 0xFF1234FF              |    |               |    |           |   |   |   |
|                     | Header Size   | 3 + size(Data Body)     |    |               |    |           |   |   |   |
|                     | Fragment ID   | Reserved                |    | Fragment Type |    | Module ID |   |   |   |
| Data Body           | SuperDrawer   | Data packet superdrawer |    |               |    |           |   |   |   |

Table 3.2: Sub-fragment packet format in the legacy system.

The sub-fragment header is an additional structure that provides detector-specific metadata for the incoming data packet. Table 3.2 illustrates an example of this header used in the legacy TileCal readout system. It includes a start marker (0xFF1234FF), the total header size (including the data payload), and

a Fragment Identifier. This identifier contains the Module ID, which specifies the corresponding superdrawer (as listed in Table 3.3), and the sub-fragment Type, which indicates the nature of the data contained in the body, detailed in Table 3.4.

| Partition | Module ID     |
|-----------|---------------|
| LBA       | 0x100 - 0x13F |
| LBC       | 0x200 - 0x23F |
| EBA       | 0x300 - 0x33F |
| EBC       | 0x400 - 0x43F |

Table 3.3: Module ID list.

| Data Element               | Sub-fragment ID |
|----------------------------|-----------------|
| Legacy Raw Data            | 0x00            |
| Legacy Compressed Raw Data | 0x01            |
| Legacy Reconstruction      | 0x04            |
| FELIX Raw Data             | 0x06            |
| FELIX Reconstruction       | 0x07            |
| FELIX Integrator           | 0x08            |
| FELIX Monitoring           | 0x09            |
| Legacy Data Quality        | 0x0A            |
| Legacy Laser               | 0x14            |
| Legacy CIS                 | 0x15            |
| TMDB                       | 0x40-0x41-0x42  |

Table 3.4: Sub-fragment ID list.

The ROD fragment is the lowest-level data structure in the ATLAS event format hierarchy. It is produced by a single ROD and contains digitized detector data. It includes both a header and a trailer. The header provides specific information, such as the run number, extended Level-1 Identifier (L1ID) (combination of the Event Counter Reset (ECR) counter and the L1ID), BCID, and L1 trigger type. The trailer contains the number of data elements and status elements, as well as their relative order.

The ROB fragment encapsulates the ROD fragment by adding its own header. It includes the ROB header, a single embedded ROD fragment, and may also contain optional status and checksum fields. The ROD fragments



are generated within the RODs of each subsystem, while the ROB fragments are assembled later in the ROS systems.

The Full Event fragment is the top-level container for all data related to an event. It contains an event header and a collection of ROB fragments. The Full Event fragment also includes event-specific information such as the event ID, run number, and trigger type. ROB fragments are the building blocks of the Full Event fragment. The Full Event fragment is build at the Event builder block of the TDAQ system. Figure 3.5 presents the described ATLAS Event Format structure used in the Tile Calorimeter legacy system, illustrating how each packet is encapsulated within the Full Fragment header.

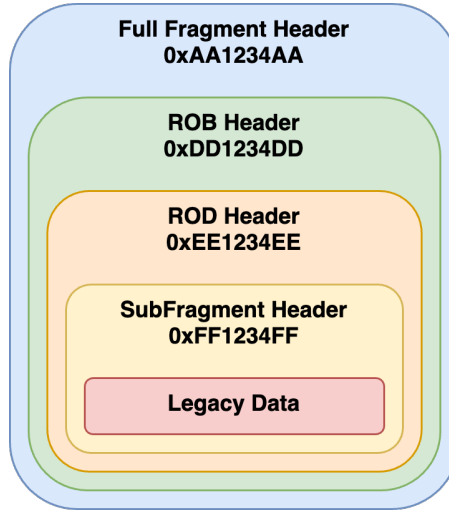


Figure 3.5: ATLAS Event Format schema for the Tile Calorimeter legacy system.

### Tile Phase-II data format

For the upgrade of the Tile Calorimeter, a new data packet has been created in order to replace the one that provides the legacy ROD. This new packet includes more information as well as more samples in the data packet. A schema of the event format for the Tile Calorimeter Phase-II upgrade can be seen in Figure 3.6.

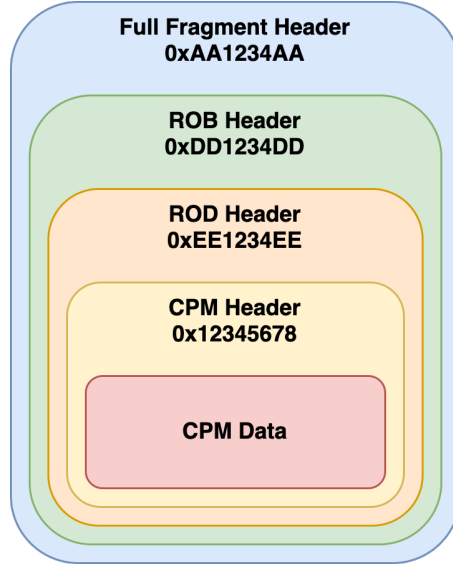


Figure 3.6: Upgraded ATLAS Event Format schema for the Tile Calorimeter Phase-II upgrade.

The data from the CPM is received in FELIX with a granularity of one packet per data type and mini-drawer. Data is packed into sub-fragments per superdrawer and data type, each having a sub-fragment header (Table 3.5) containing a start marker (0xFF1234FF), header size including data, and Fragment Identifier. As in the legacy system, the Fragment Identifier includes the Module ID (see Table 3.3) and the sub-fragment Type (shown in Table 3.4).

| Bits                |               | 31                        | 24 | 23            | 16 | 15        | 8 | 7 | 0 |
|---------------------|---------------|---------------------------|----|---------------|----|-----------|---|---|---|
| Sub-Fragment Header | Header Marker | 0xFF1234FF                |    |               |    |           |   |   |   |
|                     | Header Size   | 3 + size(Data Body)       |    |               |    |           |   |   |   |
|                     | Fragment ID   | Reserved                  |    | Fragment Type |    | Module ID |   |   |   |
| Data Body           | MD#0          | Data packet mini-drawer 0 |    |               |    |           |   |   |   |
|                     | MD#1          | Data packet mini-drawer 1 |    |               |    |           |   |   |   |
|                     | MD#2          | Data packet mini-drawer 2 |    |               |    |           |   |   |   |
|                     | MD#3          | Data packet mini-drawer 3 |    |               |    |           |   |   |   |

Table 3.5: Sub-fragment packet format.

For each mini-drawer, the data packet's contents depend on the fragment type. In this case, a raw data packet is described (see Table 3.7). Each sub-

fragment contains a header with status and configuration data. FELIX and SoftWare ReadOut Driver (SWROD) introduce two additional words: one carries status information and the packet size, while the other contains an E-Link Marker to identify the E-Link used for transmission between CPM and FELIX. The event fragment sent by the CPM is enclosed between a Header (0x12345678) and a Trailer (0x87654321). The sub-fragment ID identifies the data element in the packet (Table 3.4). The Packet Version field helps differentiate between versions of the packet, and the Module ID specifies the module (see Table 3.3). The packet also includes BCID, extended L1ID, and the mini-drawer ID, ranging from 0 to 3. The run type uses the format specified in Table 3.6, and parameters like Pedestal High Gain (HG)/Low Gain (LG) and CIS Cap/Time/Charge inform about the setup.

| Value | Description |
|-------|-------------|
| 0     | Unknown     |
| 1     | Physics     |
| 2     | LED/Laser   |
| 4     | Pedestals   |
| 8     | CIS Mono    |
| 16    | CIS Scan    |

Table 3.6: Run Type list.

Once inside the data block, two data fragments (HG and LG) are included. Each fragment contains 16 sample words per channel and gain, where each 16-bit sample word consists of 12 bits of PMT sample data (bits 11:0) and two status bits: bit 12 for Cyclic Redundancy Check (CRC) check results ('1' indicates an error) and bit 13 for ADC deserializer status on the Daughterboard.

For the integrator data, the header structure remains identical, but the data differs as we can see in Table 3.8. As the integrator readout does not go through the SWROD system, the 2 words corresponding to FELIX are not included in the data packet. Each mini-drawer transmits the integrator data for every channel (12 channels, 16 bits per channel), accompanied by 2 bits that indicate the gain of the corresponding PMT.

| Bits    |                | 31                                 | 28                | 27 | 24 | 23           | 20     | 19 | 16 | 15                             | 12                | 11 | 8 | 7              | 4   | 3   | 0 | System | Index |
|---------|----------------|------------------------------------|-------------------|----|----|--------------|--------|----|----|--------------------------------|-------------------|----|---|----------------|-----|-----|---|--------|-------|
| HEADER  | Packet Size    | SWROD Status                       |                   |    |    | FELIX Status |        |    |    | Packet Size (including Header) |                   |    |   |                |     |     |   | FELIX  | 0     |
|         | eLink Marker   | FELIX Link ID (Set from SWROD OKS) |                   |    |    |              |        |    |    |                                |                   |    |   |                |     |     |   |        | 1     |
|         | CPM SOP        | 0x12345678                         |                   |    |    |              |        |    |    |                                |                   |    |   |                |     |     |   |        | 2     |
|         | Format Version |                                    |                   |    |    |              |        |    |    | Sub-fragment ID                |                   |    |   | Packet Version |     |     |   |        | 3     |
|         | Mod/BC/MD ID   | Module ID                          |                   |    |    |              |        |    |    | BCID                           |                   |    |   | MD ID          |     |     |   |        | 4     |
|         | Extended LIID  | ECR Counter                        |                   |    |    | LIID         |        |    |    |                                |                   |    |   |                |     |     |   |        | 5     |
|         | BCR Counter    | BCR Counter                        |                   |    |    |              |        |    |    |                                |                   |    |   |                |     |     |   |        | 6     |
|         | Run Parameters | Run Number                         |                   |    |    |              |        |    |    |                                |                   |    |   |                |     |     |   |        | 7     |
|         |                | Run Type                           |                   |    |    | Pedestal HG  |        |    |    | Pedestal LG                    |                   |    |   |                |     |     |   |        | 8     |
|         |                | Fragment Size                      |                   |    |    | CIS Cap      |        |    |    | CIS Time                       |                   |    |   | CIS Charge     |     |     |   |        | 9     |
| Status  |                | CH1 Sample 2 HG                    |                   |    |    | Status       |        |    |    | CH1 Sample 1 HG                |                   |    |   |                | 10  |     |   |        |       |
|         |                | ...                                |                   |    |    |              |        |    |    |                                |                   |    |   |                | ... |     |   |        |       |
| DATA    | Status         |                                    | CH12 Sample 16 HG |    |    |              | Status |    |    |                                | CH12 Sample 15 HG |    |   |                |     | 105 |   |        |       |
|         | Status         |                                    | CH1 Sample 2 LG   |    |    |              | Status |    |    |                                | CH1 Sample 1 LG   |    |   |                |     | 106 |   |        |       |
|         |                |                                    | ...               |    |    |              |        |    |    |                                |                   |    |   |                |     | ... |   |        |       |
|         | Status         |                                    | CH12 Sample 16 LG |    |    |              | Status |    |    |                                | CH12 Sample 15 LG |    |   |                |     | 202 |   |        |       |
|         |                |                                    | ...               |    |    |              |        |    |    |                                |                   |    |   |                |     | 203 |   |        |       |
| TRAILER | CPM EOP        | 0x87654321                         |                   |    |    |              |        |    |    |                                |                   |    |   |                |     |     |   |        |       |

Table 3.7: CPM raw data packet format.

| Bits    |                | 31            | 28 | 27 | 24 | 23          | 20 | 19       | 16 | 15              | 12  | 11                   | 8 | 7                   | 4   | 3  | 0 | Who? | Index |
|---------|----------------|---------------|----|----|----|-------------|----|----------|----|-----------------|-----|----------------------|---|---------------------|-----|----|---|------|-------|
| HEADER  | CPM SOP        | 0x12345678    |    |    |    |             |    |          |    |                 |     |                      |   |                     |     |    |   | CPM  | 0     |
|         | Format Version |               |    |    |    |             |    |          |    | Sub-fragment ID |     |                      |   | Packet Version      |     |    |   |      | 1     |
|         | Mod/BC/MD ID   | Module ID     |    |    |    |             |    |          |    | BCID            |     |                      |   | MD ID               |     |    |   |      | 2     |
|         | Extended L1ID  | ECR Counter   |    |    |    | L1ID        |    |          |    |                 |     |                      |   |                     |     |    |   |      | 3     |
|         | BCR Counter    | BCR Counter   |    |    |    |             |    |          |    |                 |     |                      |   |                     |     |    |   |      | 4     |
|         | Run Parameters | Run Number    |    |    |    |             |    |          |    |                 |     |                      |   |                     |     |    |   |      | 5     |
|         |                | Run Type      |    |    |    | Pedestal HG |    |          |    | Pedestal LG     |     |                      |   |                     |     |    |   |      | 6     |
|         |                | Fragment Size |    |    |    | CIS Cap     |    |          |    | CIS Time        |     |                      |   | CIS Charge          |     |    |   |      | 7     |
|         |                |               |    |    |    |             |    |          |    | PMT Gain        |     |                      |   | Integrator data CH1 |     |    |   |      | 8     |
|         | DATA           |               |    |    |    |             |    |          |    |                 | ... |                      |   |                     | ... |    |   |      | ...   |
|         |                |               |    |    |    |             |    | PMT Gain |    |                 |     | Integrator data CH12 |   |                     |     | 19 |   |      |       |
| TRAILER | CPM EOP        | 0x87654321    |    |    |    |             |    |          |    |                 |     |                      |   |                     |     |    |   |      | 20    |

Table 3.8: CPM integrator data packet format.

## 3.2 Front-End Link eXchange

FELIX is the new common readout component developed for the ATLAS detector's Phase-II upgrade, designed to handle the increased data demands of the HL-LHC. FELIX acts as a data router, receiving packets from detector front-end electronics and forwarding them over a high-bandwidth commodity network to programmable peers for further processing.

FELIX aims to unify the detector readout process by shifting much of the data processing from hardware to software. Hosted on commodity server systems, FELIX forwards data using various network technologies such as Ethernet and RDMA over Converged Ethernet (RoCE). The primary innovation of FELIX is its ability to route detector data using programmable networked peers rather than specialized hardware, offering a flexible and scalable architecture.

FELIX employs a custom Peripheral Component Interconnect Express

(PCIe) card installed in a commodity server, which facilitates Direct Memory Access (DMA) from the front-end data into the host server's memory. From there, the data is forwarded to remote clients across the network. This design also allows bidirectional communication, enabling data flow from remote clients back to the detector front-end for control and configuration purposes. The system can support high data rates while providing scalability by distributing data across multiple servers, offering a unified and flexible platform for ATLAS readout systems.

Furthermore, FELIX is designed to handle high-bandwidth data transfers using optical links and protocols like the GBT and FULL mode, offering significant improvements in speed and data handling compared to the legacy systems.

### 3.2.1 Hardware system

Several FELIX prototypes have been developed by the TDAQ team for both Phase-I and Phase-II upgrades of ATLAS. The initial prototype used commercially available hardware, the AMD VC709 board [60]. This platform offers four optical transceivers, a AMD Virtex-7 series FPGA, and an 8-lane PCIe Gen 3.0 interface. All FELIX firmware versions are compatible with the VC-709, although it does not support 25 Gb/s links. For Phase-I, the TTC interface is provided by the TTCfx v3 FPGA Mezzanine Card (FMC) mezzanine card.

A custom-designed FELIX card for Phase-I, the FLX-712 (see Figure 3.7), was created by the FELIX team [61]. This card is equipped with a AMD Kintex UltraScale FPGA XCKU115 [62], which supports 48 high-speed optical links via Mini Parallel Optical Device (MiniPOD) transceivers and a 16-lane PCIe Gen 3.0 interface. The FLX-712 uses a removable mezzanine to interface with the Phase-I TTC system. While the FLX-712 is capable of running all Phase-II firmware variants, it cannot interface with Local Trigger Interface (LTI) nor support 25 Gb/s links [61].

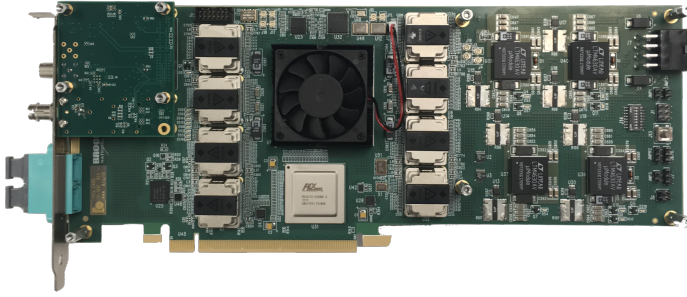


Figure 3.7: FLX-712: The FELIX Phase-I prototype design.

For Phase-II, a new prototype called the FLX-182 (see Figure 3.8) has been developed [63]. This card is based on a AMD Versal Prime VP1082 SoC [64] and uses FireFly transceivers, providing up to 24 25 Gb/s bidirectional optical links and a 16-lane PCIe Gen4 interface. The FLX-182 also includes a GbE interface and can host a DDR4 mini-DIMM memory module.

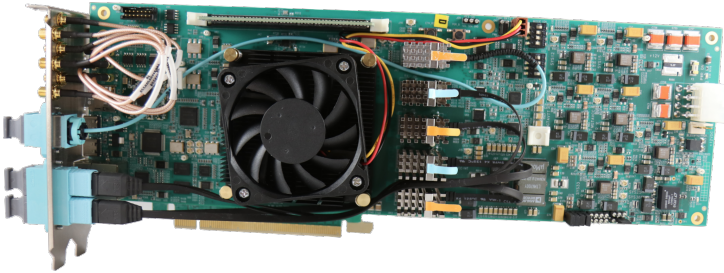


Figure 3.8: FLX-182: The FELIX Phase-II prototype design.

During the redaction of this thesis, the FELIX team is working on a new prototype for Phase-II, the FLX-155[63][65]. This card will feature an AMD Versal Premium VP1552 FPGA [66] including PCIe Gen5x16 interface capable of running at 482 Gb/s with 2x 8-lane bifurcation option and support for up to 48 bidirectional optical links.

### 3.2.2 Software system

The FELIX software suite includes a range of both high- and low-level tools designed to manage communication and data flow in the system. The primary application for handling bulk data transfer in a full-slice system is *felix-star*, which operates at the highest level. Additionally, the suite offers various command-line tools and a Graphical User Interface (GUI) for configuration and system testing [67].

Before initiating data transfer through FELIX, the input and output links need to be configured. This process is handled by the *elinkconfig* tool, a GUI-based application that enables users to compile, save, inspect, and edit the e-link configuration for any given FELIX card. This tool also allows users to write the configuration and corresponding emulator data to a selected device.

Once the e-links are configured and published into the network, applications like SWROD can connect to these e-links, enabling them to receive the data stream in real time.

#### **felix-star**

The *felix-star* architecture (Figure 3.9) serves as the central dataflow system within a FELIX setup, responsible for managing data transfers between the FELIX card and host system. In the to-host direction (CPM to FELIX), *felix-star* transmits data from the FELIX card to subscribed clients through their e-links. In the from-host direction (FELIX to CPM), messages sent through enabled e-links are transferred back to the FELIX card and onward to the front-end electronics. The configuration of these e-links, typically managed through tools like *elinkconfig*, defines the active communication pathways, which are then advertised through *felix-bus*. The *felix-bus* system consists of a hierarchical structure of JavaScript Object Notation (JSON) files, linking each FELIX host to a unique *fid*.

For seamless communication across hosts, the *felix-bus* directory must be network-accessible. The actual communication with *felix-star* is handled by

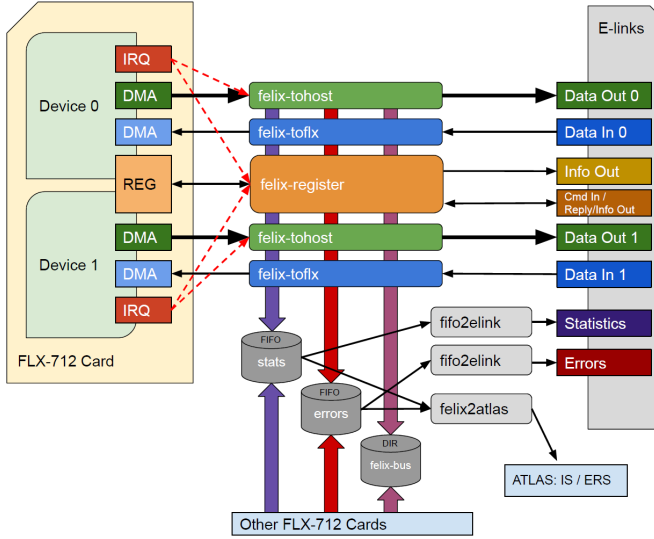


Figure 3.9: The architecture of the FELIX star application. [67]

the *netio-next* library, which uses *libfabric* to take advantage of Remote Direct Memory Access (RDMA) technology. Depending on the use case, *felix-star* can operate in buffered or unbuffered mode. Buffered mode is optimal for many small messages by combining data into pages, which are sent once a certain occupancy threshold is met or after a timeout. Unbuffered mode is ideal for high-throughput workloads, transferring large messages directly as they are received.

The *felix-star* architecture operates through independent processes responsible for dataflow management. For a single FLX-712 card setup, multiple *felix-tohost* processes can be instantiated for each DMA buffer to handle data reading and forwarding. Likewise, *felix-toflx* processes handle data transfer back to the FELIX card. These processes write statistics and errors to UNIX First In, First Out (FIFO), which can be monitored through the *felix2atlas* utility or redirected to remote clients via *fifo2elink*. Lastly, *felix-register* allows monitoring and control of FELIX firmware registers, including the card's busy status.



## Supervisor

To manage the multiple concurrent applications required to run the FELIX DAQ system, the Supervisor orchestrator is used. Supervisor [68] is a third-party process control system included in the FELIX distribution. The command *supervisord* is used to start the orchestrator, while *supervisorctl* allows users to control it. Additionally, the *felix-multivisor* utility can be used to manage multiple hosts simultaneously. The orchestration is guided by a configuration file that defines the tasks to be performed by Supervisor.

### 3.2.3 Tile Calorimeter system

The proposed configuration for the Tile Calorimeter Phase-II upgrade in USA15 is the one shown in Figure 3.10. In this configuration, there will be a need of 16 FELIX boards in total, which support 32 CPMs along with 8 TDAQi boards. Each CPM will operate with two Full Mode links, which optimizes the data transmission process. The reconstructed energy and time are encoded in 32-bit for 77 PMT channels, with an extension capability to transmit up to sixteen 12-bit samples for each of these channels, giving a total of around 15 Gbps at 1Mhz [69]. This allows the system to comfortably accommodate the bandwidth needed for both online data quality monitoring and integrator measurements.

Furthermore, each TDAQi board is configured to operate with a single Full Mode link with a bandwidth of around 7 Gbps at 1 MHz, though the system is flexible enough to easily add a second link if additional bandwidth is required. The extra bandwidth available between the CPM and FELIX systems also provides the possibility of transmitting complete L0-rawData. This improved architecture supports more detailed performance studies, including comparisons between online and offline energy reconstruction, offering a more precise and scalable solution for data processing.

| RACK 1                                                                |       |      |      |       |      |      |       |      | RACK 2                     |                      |       |      |      |       |      |      |       |  |  |
|-----------------------------------------------------------------------|-------|------|------|-------|------|------|-------|------|----------------------------|----------------------|-------|------|------|-------|------|------|-------|--|--|
| ATCA SHELF 1 - PARTITION A                                            |       |      |      |       |      |      |       |      | ATCA SHELF 3 - PARTITION C |                      |       |      |      |       |      |      |       |  |  |
|                                                                       | PPR1  | PPR2 | PPR3 | PPR4  | PPR5 | PPR6 | PPR7  | PPR8 |                            | PPR1                 | PPR2  | PPR3 | PPR4 | PPR5  | PPR6 | PPR7 | PPR8  |  |  |
| CPM1                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM1                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM2                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM2                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM3                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM3                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM4                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM4                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| TDAQi                                                                 | 1     | 1    | 1    | 1     | 1    | 1    | 1     | 1    | TDAQi                      | 1                    | 1     | 1    | 1    | 1     | 1    | 1    | 1     |  |  |
| Total Links                                                           | 18    |      |      | 18    |      |      | 18    |      |                            | Total Links          | 18    |      |      | 18    |      |      | 18    |  |  |
| FELIX occupancy                                                       |       |      |      |       |      |      |       |      |                            | FELIX occupancy      |       |      |      |       |      |      |       |  |  |
| Used links/Max links                                                  | 18/24 |      |      | 18/24 |      |      | 18/24 |      |                            | Used links/Max links | 18/24 |      |      | 18/24 |      |      | 18/24 |  |  |
| FELIX1                                                                |       |      |      |       |      |      |       |      | FELIX9                     |                      |       |      |      |       |      |      |       |  |  |
| FELIX2                                                                |       |      |      |       |      |      |       |      | FELIX10                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX3                                                                |       |      |      |       |      |      |       |      | FELIX11                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX4                                                                |       |      |      |       |      |      |       |      | FELIX12                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX SERVER1                                                         |       |      |      |       |      |      |       |      | FELIX SERVER5              |                      |       |      |      |       |      |      |       |  |  |
| FELIX SERVER2                                                         |       |      |      |       |      |      |       |      | FELIX SERVER6              |                      |       |      |      |       |      |      |       |  |  |
| ATCA SHELF 2 - PARTITION B                                            |       |      |      |       |      |      |       |      | ATCA SHELF 4 - PARTITION D |                      |       |      |      |       |      |      |       |  |  |
|                                                                       | PPR1  | PPR2 | PPR3 | PPR4  | PPR5 | PPR6 | PPR7  | PPR8 |                            | PPR1                 | PPR2  | PPR3 | PPR4 | PPR5  | PPR6 | PPR7 | PPR8  |  |  |
| CPM1                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM1                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM2                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM2                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM3                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM3                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| CPM4                                                                  | 2     | 2    | 2    | 2     | 2    | 2    | 2     | 2    | CPM4                       | 2                    | 2     | 2    | 2    | 2     | 2    | 2    | 2     |  |  |
| TDAQi                                                                 | 1     | 1    | 1    | 1     | 1    | 1    | 1     | 1    | TDAQi                      | 1                    | 1     | 1    | 1    | 1     | 1    | 1    | 1     |  |  |
| Total Links                                                           | 18    |      |      | 18    |      |      | 18    |      |                            | Total Links          | 18    |      |      | 18    |      |      | 18    |  |  |
| FELIX occupancy                                                       |       |      |      |       |      |      |       |      |                            | FELIX occupancy      |       |      |      |       |      |      |       |  |  |
| Used links/Max links                                                  | 18/24 |      |      | 18/24 |      |      | 18/24 |      |                            | Used links/Max links | 18/24 |      |      | 18/24 |      |      | 18/24 |  |  |
| FELIX5                                                                |       |      |      |       |      |      |       |      | FELIX13                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX6                                                                |       |      |      |       |      |      |       |      | FELIX14                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX7                                                                |       |      |      |       |      |      |       |      | FELIX15                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX8                                                                |       |      |      |       |      |      |       |      | FELIX16                    |                      |       |      |      |       |      |      |       |  |  |
| FELIX SERVER3                                                         |       |      |      |       |      |      |       |      | FELIX SERVER7              |                      |       |      |      |       |      |      |       |  |  |
| FELIX SERVER4                                                         |       |      |      |       |      |      |       |      | FELIX SERVER8              |                      |       |      |      |       |      |      |       |  |  |
| ILANA REQUIRES ONE LINK TO FELIX WHICH CAN BE INTEGRATED IN ANY FELIX |       |      |      |       |      |      |       |      |                            |                      |       |      |      |       |      |      |       |  |  |

Figure 3.10: Proposed distribution for the off-detector connections to FELIX cards [69].

### 3.3 Software ReadOut Driver

The SWROD is an integral component in the ATLAS data flow chain, acting as the data-handling interface between the FELIX readout system and the ATLAS HLT as shown in Figure 3.11. It replaces much of the functionality provided by the hardware-based ROD components used in Run-1 and Run-2, performing key tasks such as ROB fragment building and data formatting. The SWROD also offers buffering and HLT request processing, which was previously managed by the legacy ROS [70].

The SWROD operates through a cluster of commodity computers running multiple homogeneous software processes, all originating from the same executable, called SWROD application. These processes are configured differently depending on the data-processing requirements, such as receiving data from FELIX E-Links, applying specific algorithms for data processing, and handling HLT requests.

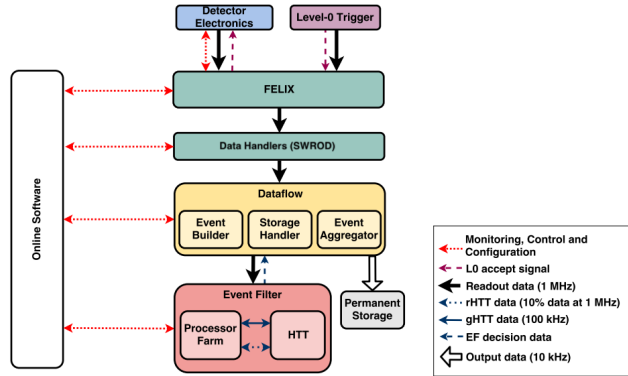


Figure 3.11: Simplified TDAQ architecture for the Phase-II upgrade, highlighting the integration points of the FELIX and SWROD systems [33].

It is fully integrated with the TDAQ online infrastructure, implementing the Run Control FSM and receiving its configuration from the standard TDAQ Configuration service. Additionally, the SWROD interacts with the Event Monitoring Sampler interface to monitor performance and publishes its statistics to the TDAQ Information Services (IS). This allows for real-time control, configuration, and monitoring of the system.

### 3.3.1 TileSWRODCustomPlugin

The SWROD application provides a framework for executing detector-specific functions required for the proper behaviour of the system. These tasks include extracting TTC information like the L1ID and BCID from incoming data packets, ensuring the integrity of these packets, and applying custom detector-specific processing to fully aggregated ROB fragments.

To perform these tasks, custom detector-specific procedures must be implemented in a shared library. This library provides three essential functions: TTC Information Extraction, Data Integrity Checking, and Custom Processing. These functions are advertised to the SWROD Application through an object of the *SwRodCustomProcessingLib* class, and are linked with each data

channel, or ROD, represented by an instance of the *SwRodDataChannel* class.

### TTC Information Extraction Function

This mandatory function extracts TTC information from data packets, such as L1ID and BCID. It takes two parameters: a pointer to the data packet and its size in bytes. The function returns a 3-tuple containing:

- A 32-bit value with the available bits of the extended L1ID.
- A 32-bit mask indicating how many bits of the extended L1ID are valid.
- A 16-bit BCID value, or 0xFFFF if no BCID is present.

The placement of these parameters is determined by the data packet sent from the CPM to FELIX, as detailed in Table 3.7. The function is capable of handling errors, throwing an *swrod::Exception* if reliable extraction is impossible. For example, if the packet is too short or corrupted, the function signals this issue.

### Data Integrity Check Function

This optional function verifies the integrity of the data packet by checking if it contains a valid checksum. If a checksum is present, the function recalculates the checksum for the packet and compares it to the stored value. If no checksum exists, the function returns *std::nullopt*. This function is only called in specific cases, such as mismatches between the data and L1A packets. Currently, no Data Integrity functions have been specified for Tile, but the system is designed to allow for future development and implementation of such functions.

### Custom Processing Function

This optional function applies detector-specific processing to the ROB fragments. It is implemented as a factory function that creates an instance of

a class inheriting from *swrod::CustomProcessor*. This processor class implements the *processROBFragment()* function, allowing for custom manipulation of the ROB fragment.

Each fragment contains attributes such as detector type, ROD version and status words [59], which can be modified by the custom processing class. The fragment's data is stored in a vector of memory blocks that can be accessed and modified as needed.

A custom processing function was developed for Tile to ensure compatibility with the legacy system. This function includes the sub-fragment data packet (see Table 3.5) into the FELIX data stream. This function is tightly integrated with the SWRODs fragment building algorithm.

The idea behind incorporating this fragment into the FELIX data is to maintain compatibility with the legacy system for testing and comparison purposes. In the legacy system, the RODs process data from the front-end electronics and append the sub-fragment header to the data packet. In the Phase-II upgrade, this sub-fragment header is technically redundant since the CPM data packet already contains all the necessary information. However, to enable seamless comparison and reconstruction between the legacy and FELIX systems, it is necessary to include the sub-fragment header in the FELIX packet. This allows existing offline reconstruction algorithms, which recognize this type of packet, to decode the data without issues.

### 3.3.2 TileSWRODFragmentSender

The *SwRodFragmentConsumer* serves as an abstract base class responsible for handling fully constructed ROB fragments. It defines several key attributes used for instantiation and operation during data processing. SWROD offers several implementations of the *SwRodFragmentConsumer* interface, configurable through their respective OKS classes:

- **SwRodFileWriter:** This consumer writes data produced by the

SWROD application into a standard ATLAS raw data file in ATLAS event format. It can operate at the level of individual ROB s or across the entire SWROD application, combining fragments with the same L1ID into a unified ATLAS event.

- **SwRodHLTRequestHandler:** Implements the HLT-to-ROS communication protocol. From the HLT perspective, a SWROD application behaves identically to a ROS.
- **SwRodEventSampler:** Creates an Event Sampler instance for the SWROD application. The Event Sampler collects fragments from all ROB s handled by the SWROD application, consolidating them into a single ATLAS event based on their L1IDs. These events are then made available to monitoring applications through the TDAQ Event Monitoring interface. Monitoring applications connect to the Event Sampler via its *SamplerType* (always set to "SWROD") and *SamplerName* (set to the ID of the respective SWROD application).
- **SwRodCustomProcessor:** This consumer applies detector-specific custom processing to fully constructed ROB fragments.

A *SWRODFragmentConsumer* named *SWRODFragmentSender* has been specifically developed for the Tile Calorimeter to maintain compatibility with the legacy system during calibration runs and testbeam campaigns during Phase-I state, as detailed in Chapter 6. In these setups, the legacy system gathers data from the front-end electronics, which is then sent to the legacy ROD system. Here, the sub-fragment and ROD fragment are appended to the data before being transmitted to the ROSEs, where a complete fragment is built, as illustrated in Figure 3.5. Subsequently, all the ROSEs are connected to the REB via a plugin called *TCPDataOut*, which transmits data through Transmission Control Protocol (TCP) packets using a specific TDAQ library. Within the REB, these packets are merged using their corresponding L1IDs

and BCIDs, sorting and combining the data into a raw packet that will be processed for offline reconstruction.

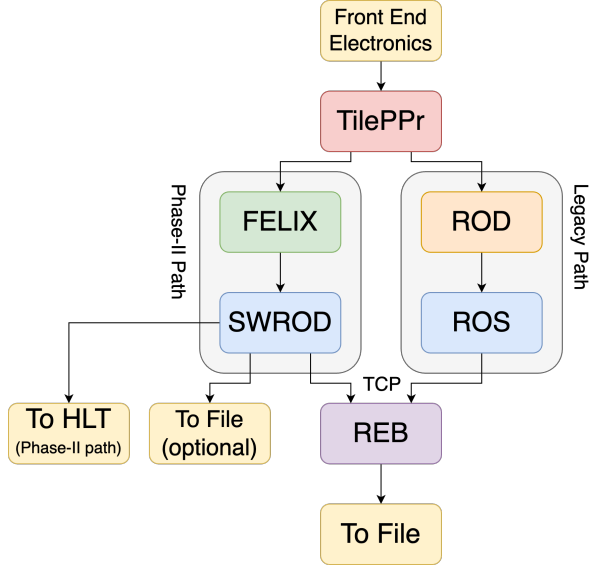


Figure 3.12: Diagram illustrating the data path readout for the Phase-II upgrade, running in parallel with the legacy data path, used for Tile standalone calibrations and testbeam campaigns.

For the Phase-I and Phase-II upgrade, the REB is deprecated, meaning modifications in the data path are required to ensure compatibility with the existing system. The upgraded system retrieves data from the new front-end electronics, with the TilePPr system receiving data through the CPM. This data is packaged as shown in Table 3.7 and sent to the FELIX system, which routes the packet to the SWROD system via FELIX e-links. As previously explained, the SWROD system appends the sub-fragment header. While SWROD can send data to the HLT via the *SwRodHLTRequestHandler* or save it using the ATLAS event format through the *SwRodFileWriter*, it does not natively support transmitting data via TCP to the REB.

To bridge this gap, a custom *SWRODFragmentConsumer* was developed, inspired by the legacy TDAQ system’s *TCPDataOut* code. This consumer adds the headers corresponding to the full fragment packet, encapsulates the whole

data packet, divides the data into chunks and forwards it to the REB. The configuration of data destinations, port, and buffer settings has been integrated into the OKS system, providing a more efficient way to manage these settings. Figure 3.12 illustrates the readout process using the Phase-II electronics.

### 3.4 TileFelixIntegrator Readout

The integrator readout integrates the current from the PMTs for the calibration of the calorimeter using a Cesium-137 source. In addition to calibration, it also offers a relative measurement of the accelerator’s luminosity at the ATLAS interaction point. The integrator readout employs six distinct gains, which enables it to accurately cover a dynamic range of eight orders of magnitude in luminosity measurements, spanning from specialized procedures like the van der Meer scan to the collection of physics collision data [71].

The integrator readout integrates the current from the PMTs for the Cesium calibration runs, which are used to calibrate the TileCal cells and normalize the gains of the PMTs [46]. Another function of the integrator is to measure the anode current induced by MB proton-proton interactions. These signals, which result from inelastic collisions, allow for continuous monitoring of variations in the calorimeter’s response over extended periods. Additionally, the MB signal is utilized to monitor relative luminosity within the system [72].

In the upgraded Tile Calorimeter system, the TilePPr is capable of transmitting integrator data via two methods. Before FELIX was implemented, the integrator readout data was transmitted through the IPbus system [73], with the CPM sending the data across the network. This data was captured by dedicated software for storage and later reconstruction. With the introduction of FELIX, the data is now transmitted through a dedicated set of e-links. Since this readout process is independent of triggers and is used for parallel data analysis, it bypasses SWROD and directly saves the data for subsequent reconstruction and analysis.



The integrator data transmission was first demonstrated using FELIX developer tools, such as *fdaq*, which directly captured data from the e-links. Later, this process was streamlined with custom scripts for tasks like Cesium scans and data collection during regular operation. These scripts were eventually integrated into the TDAQ system. Although using scripts proved functional, the need for a standardized, reliable method led to the development of a dedicated C++ library, *TileFelixIntegrator* library. This library supports both standalone readout (e.g., for Cesium scans) and MB readout via TDAQ software, employing the FSM for smooth operation and control.

### 3.4.1 TileFelixIntegrator Library

This library has been designed to establish connections with the hardware, collect incoming data, process it, and save it to a file. It operates within a highly event-driven and multithreaded environment to ensure efficient handling of large data volumes. It has been designed using the *felix-client-thread* library provided by the FELIX team. The *felix-client-thread* library serves as an interface for users to communicate with FELIX systems over a network. This library provides a simplified and efficient user interface by exposing a set of methods and hooks for callbacks, which abstract the complexity of the lower layers of the system. Methods can be directly called by the user to perform various operations, such as sending messages. Additionally, callbacks, defined by the user, are triggered asynchronously in response to specific network events [74].

The software starts by initializing itself and setting up a series of callbacks. These callbacks are functions that respond to specific events, such as when data is received, a connection is established, or the system is initialized. This event-driven design allows the system to react dynamically to the state of the hardware and incoming data streams.

Once initialized, the system must be configured with specific parameters like the Internet Protocol (IP) address, log level, and file paths. These settings

are passed through a configuration object that defines the properties needed to communicate with the hardware. After this, the system opens an output file for data storage and establishes subscriptions to data channels. These channels dictate which specific streams of data the system will monitor and collect.

When data starts arriving from the hardware, the software processes it by updating statistics on how many messages have been received, whether any data was truncated, and if there were any errors. The data is then stored in a queue, ready to be written to the output file. This writing process occurs in a separate thread, allowing the system to handle incoming data concurrently without slowing down the main data collection tasks.

Data collection is carefully controlled to ensure smooth operation. The system can start and stop data collection based on specific triggers. When data collection begins, a dedicated thread is created to manage the incoming data, and when it ends, the system unsubscribes from the data channels and ensures that all remaining data is written to the file before closing it. This approach prevents data loss and ensures that everything is properly saved.

In addition to data handling, the system also manages connections to the hardware. When a connection is established or lost, the system logs these events and keeps track of how many connections are active. This is important for monitoring the health and stability of the data acquisition process.

The configuration of the system is flexible and can be adjusted through a separate class that holds all the necessary parameters. This makes it easy to update settings like the hardware's IP address, logging preferences, and file paths, allowing the integrator to adapt to different environments or hardware setups.

### **TDAQ version**

This module is integrated into the TDAQ software (see Figure 3.13) follows the FSM of the system, handling transitions between states. Its primary function

is to manage the interaction between TDAQ and FELIX integrator library, ensuring smooth state transitions and efficient data handling.

The module is initialized with null pointers, preparing it for configuration. During setup, it retrieves essential parameters like the Module ID, IP address, and subscriptions from the OKS database. This information is stored in a configuration object, which sets up the FELIX system for data collection. The module also establishes communication with the IS, which will be used to gather and publish metadata during runs.

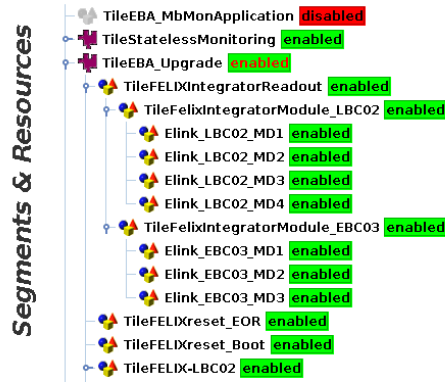


Figure 3.13: Tile Integrator module integrated into the TDAQ software for the testbeam partition, showing the list of e-links corresponding to the various mini-drawers.

In the CONFIGURE state, the module uses the configuration object to set up the FELIX integrator, ensuring that all necessary parameters are in place. If successful, the module transitions to the CONFIGURED state, ready for data acquisition. When transitioning to the START state, the module begins data-taking by activating the FELIX integrator, marking the system as RUNNING. Data is collected and processed, adhering to the real-time performance needs of TDAQ.

In the STOP state, data collection is halted, and run metadata, such as the run number, is retrieved from the IS. The output data file is renamed to include the run number, ensuring it is properly labeled. The module then publishes

session statistics, such as message counts and error rates, and transitions back to a non-ready state, requiring reconfiguration for future runs.

Throughout its lifecycle, the module manages state transitions like connecting, stopping high-level tasks, and archiving data. All transitions are logged for transparency. The module also provides a user interface for commands, supports clearing information, and retrieves statistics, giving operators insight into system performance.

### Standalone version

For the standalone version, which will be used mainly for Cesium scans), the program uses Boost [75] to parse command-line arguments, allowing users to configure the IP address, logging level, output file paths, e-links to connect and TileCal module type (LB or EB). It also dynamically generates file names based on the current time to ensure unique outputs for each run.

After configuration, the program starts data-taking. If no iteration limit is set, it runs continuously until stopped by the user. Otherwise, it is designed to stop after the specified number of iterations. A signal handler listens for *SIGINT* (Ctrl+C) to safely stop data-taking. When data-taking ends, the program halts the integrator, prints run statistics, and shuts down gracefully, saving data and releasing resources.

### Data reconstruction

A software was developed in order to process the data coming from FELIX integrator readout files. It reads binary data, synchronizes packets, processes it, and saves the results in a *ROOT* file for further analysis. *ROOT* is a data analysis framework widely used in high-energy physics, developed at CERN [76]. It allows users to store and analyze large volumes of data in a structured format. *TTree* structure from *ROOT* software is used, which is highly efficient for storing and accessing large datasets. This script uses *ROOT* to create files that hold the processed data from FELIX, which can then be used for further

analysis in physics experiments. The software ensures proper reconstruction of events by handling data synchronization and error correction.

The software begins by verifying user inputs for the module type (LB or EB) and the run number or timestamp. Based on this, it searches for the appropriate data file in predefined directories. If no file is found matching the criteria, the software exits with an error.

The script reads binary data from FELIX files in chunks of 4 bytes. It looks for specific packet markers (start and end of packet) and extracts necessary information such as the Module ID, L1ID, and Bunch Crossing Reset (BCR) counters. To ensure synchronization between data packets, the script adjusts BCR values when mismatches are detected.

After processing, the script creates a *ROOT* file, which acts as a container for the data. Inside this file, a *TTree* structure is created, and various branches are defined to store relevant data like PMT gains, BCID, L1ID, and event timestamps. As data is processed, it is stored in the appropriate branches of the *TTree*.

As the script processes each packet of data, it fills the *ROOT* tree with the extracted information. The data is grouped by module ID, and synchronization between different data streams is ensured using BCR counters. The script includes mechanisms for handling errors, such as packet repetition or invalid BCR values. Once the data for a module is processed, the corresponding branches in the *ROOT* tree are updated with the packet values.

After processing all the data, the script writes the filled *ROOT* tree to a file, which is saved in a predefined directory with a name that includes the run number and module type. This *ROOT* file contains all the processed data in a structured format that is ready for analysis.

Chapter 6 presents results obtained using this software during various test-beam campaigns.



## Chapter 4

# Developments for the Tile Computer-on-Module

*This chapter presents the development of the TileCoM, a compact System-on-Chip based module designed to monitor and control the TileCal on-detector and off-detector electronics. It details the hardware, firmware, and software components, including the boot process, use of PetaLinux and AlmaLinux, and integration of GitLab CI/CD pipelines. Additionally, it describes the implementation of IPbus and OPC UA protocols for real-time monitoring and data publication to the ATLAS DCS.*

The TileCoM is a compact, high-density SoC module integrated into the TileCal system for monitoring and control tasks. It provides remote access to the TilePPr system, enabling system health checks, FPGA programming, and local clock distribution. Additionally, TileCoM allows for continuous monitoring of DCS sensors across the TileCal infrastructure, ensuring robust detector operation and real-time adjustments as needed.

## 4.1 Hardware

A SoC is an integrated circuit that combines multiple components of a computing system into a single chip. It is designed to perform complex tasks by combining diverse functionalities such as processing, memory, communication, and control in a compact and power-efficient form factor.

A SoC refers to integrating multiple essential components of a computing system onto a single silicon die. This includes one or more Central Processing Units (CPUs), RAM, nonvolatile memory, and various peripheral devices, all consolidated into a unified chip. When the silicon die incorporates a FPGA alongside an embedded CPU, such as an Advanced RISC (Reduced Instruction Set Computer) Machines (ARM) core, it becomes a reconfigurable SoC. This configuration combines the flexibility of programmable hardware with the processing capabilities of embedded cores, creating a compact and versatile system capable of handling diverse computing tasks efficiently [77].

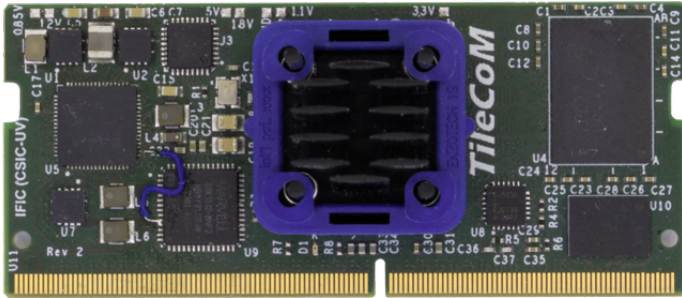


Figure 4.1: Picture of the TileCoM board version 1.2.

The TileCoM (Figure 4.1) is a specialized SoC module designed at Institut de Física Corpuscular (IFIC) to support the operation, monitoring, and control of the TileCal calorimeter system. It integrates a range of high-density components on a compact Printed Circuit Board (PCB) measuring 3 x 7 cm and manufactured with 10 layers of Flame Retardant 4 (FR4). The hardware is based on the Advanced Micro Devices (AMD) Zynq UltraScale+ ZU2CG



SoC [62], which combines an ARM Cortex-A53 processor and programmable logic.

The TileCoM module is powered by a Texas Instruments TPS6508641 [78] Direct Current to Direct Current converter (DC-DC) converter, which is configured to meet the specific power sequencing requirements outlined in the datasheet for the Zynq UltraScale+ architecture. This converter ensures stable and efficient power delivery across the module, adhering to the precise voltage and timing needs of the system components.

The TileCoMs memory and storage capabilities include 2GB of DDR4 RAM (Micron MT53D512M32D2DS-053 [79]), a Quad Serial Peripheral Interface (QSPI) memory (Micron MT25QL256ABA8E12 [80]) for boot purposes, along with a microSD slot, used for supplementary storage and boot, including configuration files and firmware updates.

The TileCoM module features some GbE interfaces for network communication. One of the GbE connections utilizes the Multi-Gigabit Transceiver (MGT) from the Processing System (PS) section of the Zynq UltraScale+, which connects through a GbE switch to the ACBB and subsequently to the Zone 2 connector. The second GbE connection interfaces with the Marvell 88E1512 [81] PHY chip on the TileCoM, linking through the ACBB to the Zone 3 connector. Additionally, a variety of interfaces, including Universal Serial Bus (USB) (via the Microchip USB3320 [82]), Serial Peripheral Interface (SPI), I2C, and Universal Asynchronous Receiver/Transmitter (UART) (configured through the Zynq UltraScale+), support communication with various peripheral devices.

The module also provides a set of General Purpose Input/Output (GPIO) pins operating at 1.8V logic levels, enabling versatile I/O interactions with various components in the system.

The TileCoM is equipped for local clock recovery and generation using the Skyworks Solutions SI5338C [83] clock generator. This clock generator allows for flexible frequency synthesis and jitter attenuation. The generated

clock signals are then distributed via the Renesas 854S006 [84] Differential-to-LVDS fanout buffer, which ensures low-skew and low-jitter clock distribution to multiple components within the TilePPr system.

## 4.2 Firmware

The firmware for the TileCoM has been developed using the Vivado toolset from AMD [85]. The design incorporates the PS block through the integration of the Zynq UltraScale+ Multiprocessor System on Chip (MPSoC) Intellectual Property block (IP block), which manages all related configurations and connections. An I2C interface has also been implemented in the Programmable Logic (PL) section, using the Advanced eXtensible Interface (AXI) interconnect to enable communication between the PS and PL. This I2C line will be used to interface with the IPMC on the ACBB in order to retrieve key information, such as the slot number of the ACBB within the ATCA shelf. Additional signal lines and interfaces necessary for the ACBB functionality will be implemented following full system debugging. The firmware design is modular and extensible, allowing for further developments to support all the required functionalities of the TileCoM.

## 4.3 Software

Since the TileCoM handles communication with the DCS system, a Linux-based operating system provides a robust and convenient environment for development and integration. To achieve this, several system components must be properly configured. The first step is setting up the bootloader, which ensures the correct initialization of the hardware and prepares the system for booting a Linux distribution. Once configured, the next stage involves TileCoM to successfully load and run the chosen Linux environment.

### 4.3.1 Booting Stages

The Zynq MPSoC boot process [86], illustrated in Figure 4.2, follows a structured multi-stage sequence to initialize and configure the system. It supports various boot modes, including secure and non-secure options, and allows versatile operation of its PS and PL components.

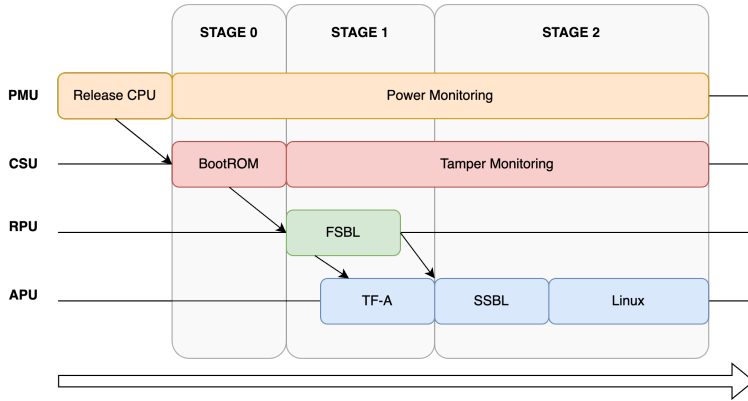


Figure 4.2: Boot flow for the Zynq UltraScale+ MPSoC (based on [86]).

The boot process begins with Stage 0 (BootROM), where the BootROM detects the boot mode and loads the First Stage Boot Loader (FSBL). The Zynq MPSoC supports multiple master boot methods, including QSPI, Not AND (type of flash memory) (NAND), Secure Digital (SD), and embedded MultiMediaCard (eMMC), for both secure and non-secure operation. Additionally, slave boot methods, such as Joint Test Action Group (JTAG) and USB 2.0, are supported for debugging and development. Once detected, the FSBL is loaded into the On-Chip Memory (OCM) by the Configuration Security Unit (CSU) after being released from reset by the Power Management Unit (PMU). The PMU, running in server mode, simultaneously monitors power while the FSBL initializes.

In Stage 1, the FSBL is executed from the Application Processing Unit (APU) or Real-time Processing Unit (RPU) and is responsible for initializing processor resources, reading header blocks in the boot media, and loading

programs into appropriate memory locations for different processors. The FSBL also handles secure boot operations if configured. On the APU, after the FSBL completes its tasks, it hands control to Trusted Firmware-A (TF-A). TF-A further passes control to a Second Stage Boot Loader (SSBL), such as U-Boot, to start the Stage 2.

Stage 2 begins with the execution of U-Boot, which is typically loaded into external memory by the FSBL. U-Boot is responsible for loading the operating system (e.g., Linux) from flash storage or PCIe and passing control to the Operating System (OS) image. U-Boot facilitates communication between the bootloader and the Linux kernel by providing necessary boot arguments or device tree configurations.

Finally, the Linux Kernel and Init Process are loaded and executed. The kernel initializes the hardware, mounts the root file system, and prepares the environment for application execution. After kernel initialization, startup scripts are executed to launch application-specific processes, with the terminal console usually being the first program to run.

### **FSBL modification**

To utilize the PS-Gigabit Transceiver (GTR) block, which manages in our case the Ethernet connection in the PS, a 125 MHz input clock is required. This clock signal must be provided to the PS through dedicated ports. The TileCoM includes a 25 MHz crystal oscillator that serves as an input to the SI5338 clock generator, which produces the necessary 125 MHz clock signal for the system.

The SI5338 must be configured prior to the PetaLinux kernel initialization to ensure proper network functionality. If the SI5338 is configured after the kernel has started, the network card will fail to initialize, rendering Ethernet connectivity unavailable.

To address this requirement, the FSBL code was modified to perform the configuration of the SI5338 via I2C during the boot process. The FSBL ap-

plies the required register settings, which are generated using the Skyworks ClockBuilder Pro software, ensuring the proper clock configuration before the kernel begins its operation.

### 4.3.2 PetaLinux

PetaLinux [87] is a build system to facilitate the development and deployment of Linux-based systems on SoC platforms such as the Zynq UltraScale+. It builds on the capabilities of the Yocto Project.

The Yocto Project [88] is an open-source initiative that provides a flexible framework for building custom Linux distributions tailored to specific hardware platforms. It uses a highly configurable build system based on BitBake [89] and a collection of metadata, recipes, and layers. These elements allow to define the packages, configurations, and kernel features needed for embedded systems.

PetaLinux provides a comprehensive build system equipped with command-line and menu-driven tools for creating embedded Linux images. It includes source code, libraries, applications, and Yocto recipes for various hardware drivers, traditional Linux applications, and utilities, effectively managing Linux kernel sources and libraries. The integration with Vivado hardware designs enables PetaLinux device drivers to work seamlessly with Vivado IP blocks, allowing the import of hardware designs into the PL.

PetaLinux supports multitasking on the Zynq MPSoCs APU cores, delivering fast processing capabilities but lacking real-time functionality. For real-time applications, the R5 cores can be utilized with an Real-Time Operating System (RTOS) like FreeRTOS [90], and communication between the A53 (PetaLinux) and R5 cores can be achieved using OpenAMP [91].

The system uses a device tree to define the hardware configuration of the Zynq MPSoC. This configuration, written in Device Tree Source (DTS) files, is compiled into a Device Tree Blob (DTB) and linked into the kernel image. Additionally, PetaLinux leverages the Yocto ecosystem, supporting the

integration of Yocto-generated Red Hat Package Manager (RPM) feeds and offering robust revision and source control capabilities.

### 4.3.3 AlmaLinux

AlmaLinux has been adopted as the primary operating system at CERN, as CentOS 7 reached its End-of-Life [92]. Due to this transition and additional security considerations, the use of PetaLinux is no longer permitted within the ATLAS system. To accommodate AlmaLinux 9 on the TileCoM, a specialized script developed by the SoC group at CERN is employed.

This script automates the creation and configuration of a root filesystem tailored for ARM-based systems, such as those used in the TileCoM. It simplifies the process of preparing a compatible root filesystem by integrating cross-architecture support, software installation, and system configuration into a single streamlined workflow. By using Quick Emulator (QEMU), the script allows for cross-architecture operations, enabling it to run on host machines with a different architecture from the target ARM system. Furthermore, the script was extended to include the installation of additional required packages, configure the network settings, and create a dedicated user for the system, providing a ready-to-use image with all the tools

However, despite this progress, the PetaLinux project remains a necessary component of this approach. The kernel generated by PetaLinux is still required for integration with the AlmaLinux root filesystem. As of the time of writing, no alternative method exists to achieve this configuration without relying on the PetaLinux kernel.

### 4.3.4 Continuous Integration

To maintain organization, structure, and efficiency in the TileCoM project, Git is used for version control, tracking all changes and development branches. Git [93] is a distributed version control system designed to manage source code

changes in software development. For this project, GitLab [94] serves as the primary platform, providing repository management, issue tracking, and other developer features.

Two Git repositories were established for TileCoM: one dedicated to hardware development (Vivado design) and another for software development (operating system). To automate the build process, GitLab Continuous Integration / Continuous Deployment (CI/CD) is implemented. GitLab CI/CD is a built-in automation tool in GitLab that helps streamline software development by automating code building, testing, and deployment. This automation ensures consistency in the build process, mitigating errors caused by outdated dependencies or compatibility issues. The execution of the CI/CD pipelines is handled by a GitLab Runner, which is an application that executes the defined jobs in the pipeline. The runner is configured in a dedicated server with all the necessary environments and tools, including Docker containers, to ensure reproducibility and isolation during the build processes.

In the hardware repository (Vivado design), a CI/CD pipeline is configured to generate the hardware description files required for PetaLinux to create the operating system images. This process runs within a Docker container. Docker [95] is a containerization platform that allows to package applications and dependencies into lightweight, portable containers. These containers ensure that software runs consistently across different environments. This Docker container includes a preconfigured Vivado image to synthesize, implement and export the hardware configuration. Once the hardware files are generated, the pipeline automatically pushes them to the software repository, triggering the corresponding CI/CD workflow in the software repository.

The software repository, which contains the operating system, includes a CI/CD pipeline configured to retrieve the hardware files from the corresponding hardware repository and build the system image using PetaLinux tools. This entire process is performed with a runner using Docker. In addition, the pipeline is also set up to generate operating system files for an AlmaLinux

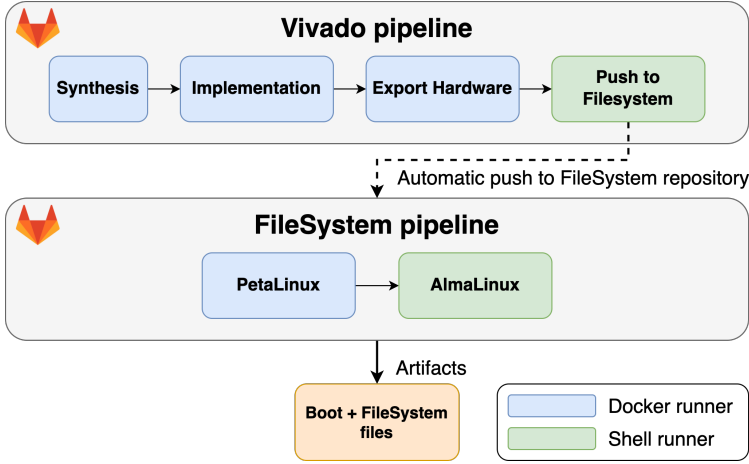


Figure 4.3: Diagram illustrating the complete CI/CD workflow implemented for the TileCoM repositories.

image using a shell runner, following the procedure described in the previous subsection.

Figure 4.3 illustrates the pipelines for both the Vivado hardware build and the file system generation.

## 4.4 Control and monitoring

The primary function of TileCoM is to collect the status from on- and off-detector components and transmit it to the ATLAS DCS. To achieve this, a dedicated monitoring framework has been developed. This framework integrates the necessary driver interfaces for hardware communication, an Open Platform Communications Unified Architecture (OPC UA) server for standardized data exchange and the IPbus protocol to facilitate communication with the CPMs.

### 4.4.1 IPbus

The IPbus protocol is a lightweight, packet-based communication protocol developed to facilitate the control and monitoring of memory-mapped resources



in FPGA-based hardware systems. It enables efficient Ethernet-based communication between software running on control computers and the hardware devices, providing a reliable and scalable solution for configuring registers, reading sensor data, and performing diagnostics in complex data acquisition systems [73].

TileCoM integrates IPbus connectivity to access and interact with all CPMs, enabling the retrieval of data from internal sensors as well as monitoring information from the front-end electronics to be published later via OPC UA.

#### 4.4.2 OPC UA

OPC UA [96] is a platform-independent, service-oriented framework designed for secure, reliable, and scalable industrial communication. It is widely used in industrial systems to facilitate data exchange and interoperability between devices, applications, and systems across diverse hardware platforms and operating systems.

In ATLAS, OPC UA facilitates communication between the supervisory control layer and various hardware components. This includes managing distributed I/O boards and embedded devices that operate over the CANopen protocol [97].

The OPC UA servers for TileCoM are implemented using the Quasar framework [98], which provides tools and abstractions that simplify the creation of OPC UA servers. The process begins with designing a device-specific, object-oriented information model, from which the server code is automatically generated. This generated code is then integrated into the TileCoM monitoring application, enabling the OPC UA interface. As a result, any OPC UA-compatible client can subscribe to and retrieve the published data seamlessly.

For the Tile Calorimeter system, two OPC UA servers will be implemented. The first server will monitor the health of the TilePPr system, collecting data from various sensors on the ACBB board, CPMs, and TDAQi. This infor-

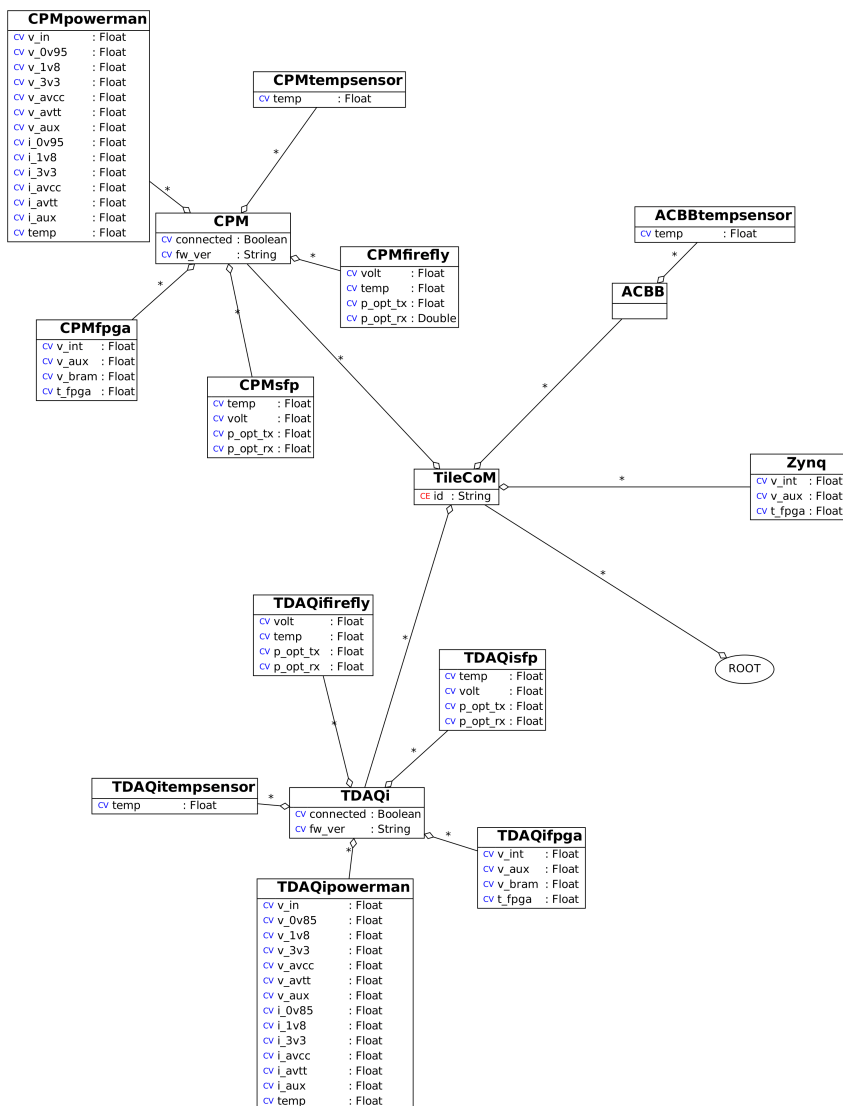


Figure 4.4: Hierarchical representation of datapoint elements and their associated types, generated using the Quasar framework for the TileCoM off-detector monitoring.

mation will be directly retrieved from the TileCoM. The second server will focus on monitoring the mini-drawers, with data being accessed through dedicated memory locations in the CPM, where the monitoring information from the mini-drawers is stored. Figure 4.4 presents the current on-development OPC UA diagram for the off-detector electronics.

According to the design, the TileCoM serves as the central node, interfacing with all other devices. The ACBB node retrieves information related to the board's status, such as the temperature sensors embedded on the PCB. The CPM and TDAQi nodes are responsible for collecting measurements from various components, including temperature sensors, power management units, and optical devices. This includes parameters such as the optical power levels of the transceivers. The design remains under active development, and additional classes and configurations will be introduced throughout the debugging phase.

The OPC UA server has been programmed to support communication with various devices over IPbus, utilizing configuration files and register mappings to access monitoring and status data. This integration enables the server to retrieve information directly from hardware components in real time. To visualize the data published by the OPC UA server, a test setup was created to receive and plot the information using Grafana [99], an open-source analytics and visualization platform. In this setup, the OPC UA server streams data to a database hosted on InfluxDB [100], a high-performance time-series database optimized for storing and querying temporal data efficiently. To bridge the OPC UA server and the InfluxDB instance, Telegraf [101] is used as the intermediary. Telegraf is a lightweight, plugin-driven server agent for collecting and sending metrics from various sources to supported outputs, including InfluxDB. It includes an OPC UA input plugin, which enables it to subscribe to specific nodes on the server and periodically collect their values.

Figure 4.5 shows sample plots generated through this setup, illustrating real-time monitoring of the CPM FPGAs internal temperature and voltage

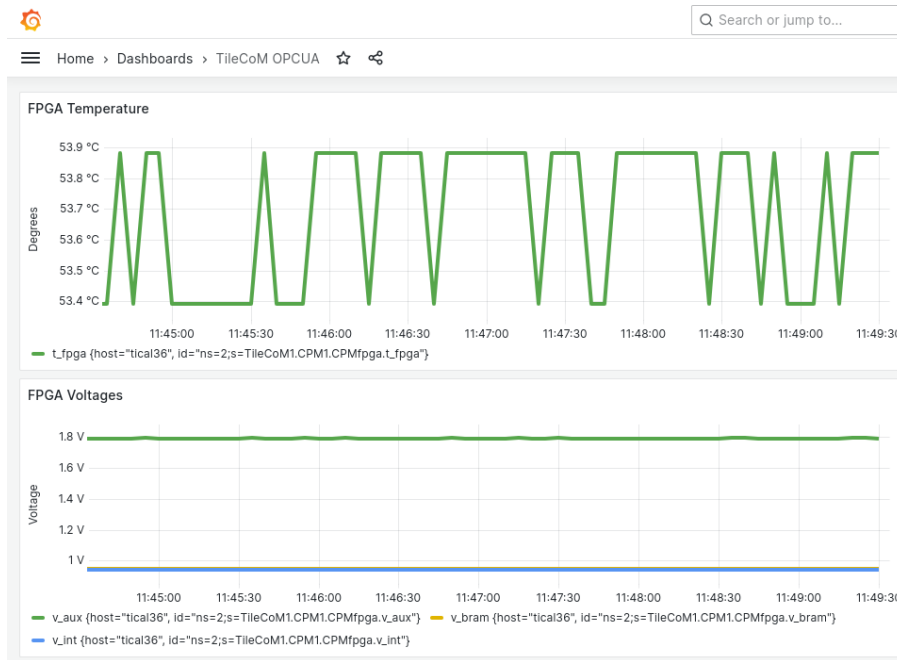


Figure 4.5: Real-time monitoring of the CPM FPGA using Grafana. The upper plot displays the internal FPGA temperature retrieved via OPC UA. The lower plot shows the auxiliary, BRAM, and internal voltage rails of the FPGA.

levels.

At the time of writing this thesis, the limited availability of hardware prevented the acquisition of data from additional devices. As a result, only internal measurements from the CPM FPGA are available on the OPC UA server, which nonetheless confirms the correct operation of the server.

Additionally, a known issue in the current version of the TileCoM hardware—specifically, data transmission errors when installed inside the ACBB board due to layout problems in the TileCoM—has constrained testing. Consequently, all TileCoM tests have been conducted using the TileCoM Mother-Board, a dedicated debugging board that allows for independent power supply and reduced noise, enabling reliable data reception. A new hardware revision addressing these issues is underway at the time of writing.

## Chapter 5

# Design of the ATCA Switch Board

*As discussed in the previous chapter, the TileCoM must efficiently transmit a significant amount of information across the network. This is achieved using the ATCA infrastructure, which facilitates communication between all TilePPr modules housed within a shelf. This chapter presents a detailed overview of the design, development, and implementation of the ATCA switch board, debugging operations and results of performance tests.*

When all the TilePPr modules are installed in an ATCA shelf, a robust mechanism is required to enable communication with these boards. This includes accessing DCS information, performing configurations, and monitoring the system. To facilitate these operations, a high-speed switch is necessary to interconnect all the TilePPrs inside the ATCA shelf.

This interconnection is made possible through the ATCA standard. The ATCA standard defines a framework for integrating and connecting high-performance boards within a shelf using a unified backplane.

## 5.1 The ATCA standard

The ATCA was developed by the PCI Industrial Computer Manufacturers Group (PICMG)[102] to address the increasing demands for modular, scalable, and high-reliability computing solutions. The ATCA specifications, also known as PICMG 3.x , is a high-performance, open standard for the design of computing systems, particularly in telecommunications and other mission-critical applications [103].



Figure 5.1: An 14-slot ATCA shelf from the Schroff nVent vendor.

ATCA supports high-performance interconnects like 10GbE and PCIe, making it suitable for data-intensive applications. Its modular architecture, using pluggable boards called blades, allows for easy upgrades and scalability to meet evolving requirements. Additionally, ATCA systems are designed with reliability in mind, incorporating features like redundancy, hot-swappable components, and fault-tolerant designs to ensure minimal downtime. These systems also comply with standardized mechanical, electrical, and software specifications, ensuring compatibility across components from different manufacturers. Beyond telecommunications, ATCA is widely used in scientific research, particularly in High Energy Physics (HEP) experiments such as those conducted at CERN [104].

### 5.1.1 Connectivity

The ATCA standard provides a well-defined structure for connecting boards within an ATCA shelf (Figure 5.1). Boards interface with the back-plane using specialized connectors referred to as Zones (see Figure 5.2), which are responsible for various functionalities:

- **Zone 1 (Management and Power):** Located at the bottom of the ATCA back-plane, the Zone 1 connector is responsible for delivering power and enabling management capabilities for the boards.
- **Zone 2 (Base and Fabric Interfaces):** The Zone 2 connector facilitates communication through the Base and Fabric Interfaces. These interfaces are needed for high-speed data exchange between the boards within the shelf.
- **Zone 3 (Rear Transition Module):** The Zone 3 connector provides an interface between the main board and the RTM. This zone is used for additional inputs/outputs and connections specific to the application requirements, enhancing the modularity and scalability of the system.

All ATCA back-planes are equipped with a dual-star base interface network. The base interface primarily utilizes 1000BASE-T (Gigabit Ethernet) and is structured such that logical slots 1 and 2 serve as the hubs of the dual-star configuration. In a typical 14-slot ATCA shelf, these slots are generally allocated for switch blades, while the remaining slots (3-14) are designated for processor nodes.

For high-speed data transmission, the back-plane utilizes a fabric interface. The fabric interface is available in two main configurations: full mesh and dual-star. Unlike the base interface, the fabric interface does not impose a specific data protocol [106]. Each channel in the fabric interface consists of four bidirectional 100-ohm differential pairs. Signal levels, data rates, and encoding are left for the user to define. Over successive generations, the performance

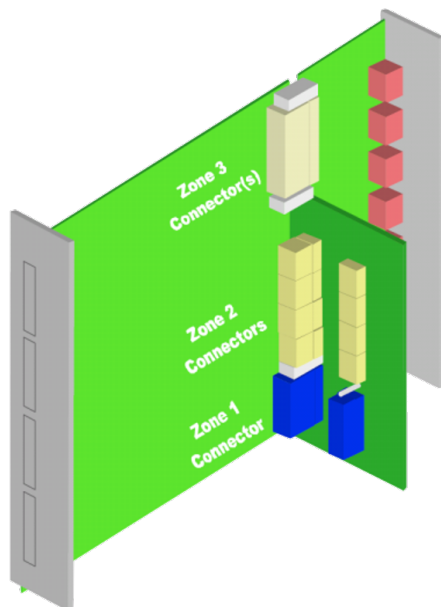


Figure 5.2: Diagram of an ATCA board connecting to the ATCA shelf backplane [105].

of the fabric interface has significantly increased, advancing from 10G (2.5 Gigabits per second (Gbps)  $\times$  4) to 40G (10 Gbps  $\times$  4), and now reaching 100G (25 Gbps  $\times$  4) [106].

### 5.1.2 ATCA Link Board

An ATCA link board was developed by IFIC personnel as a first approach in order to communicate all the TilePPr connected in the ATCA shelf (see Figure 5.4). When installed in Slot 1 or Slot 2 of the ATCA shelf, this board acts as a concentrator for all the slots in the shelf using the Base Interface. The front panel of the board features 14 Registered Jack 45 (RJ-45) connectors, each corresponding to one of the slots in the ATCA shelf. To connect to a specific slot, a cable must be manually plugged into the designated connector on the link board.

To establish communication across all slots, an external switch is required,



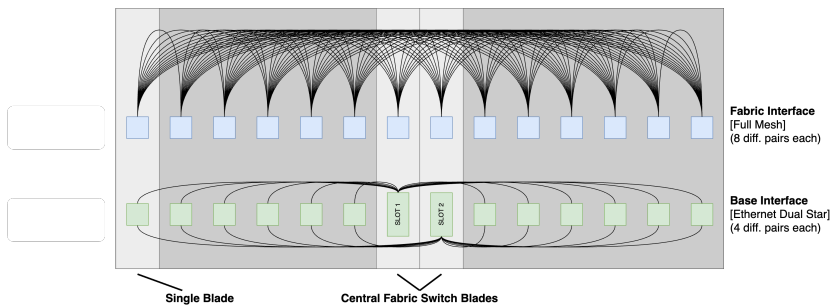


Figure 5.3: Diagram of a 14-slot ATCA back-plane interface connections.

which significantly increases the number of cables. This is further compounded by the cables needed to connect the front-end electronics to the TilePPr. As a result, this setup demands an extensive and cumbersome cable infrastructure.

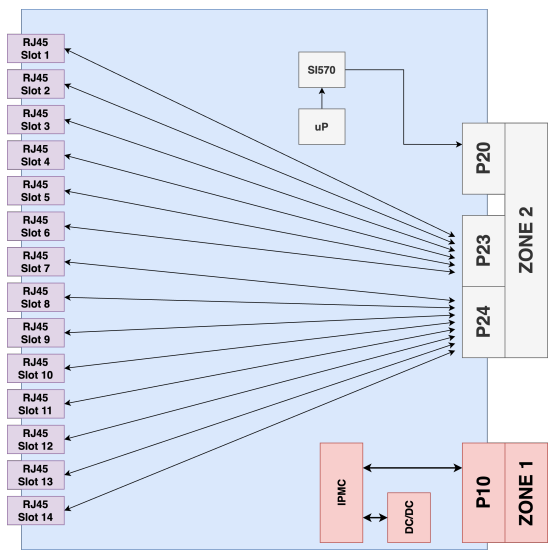


Figure 5.4: Block diagram of the ATCA link board design. This approach requires a dedicated Ethernet cable for each ATCA slot to establish communication with the corresponding board.

## 5.2 ATCA Switch Board

To address the limitations of the ATCA link board, a dedicated ATCA switch board solution was proposed. This board functions as a fully integrated switch, enabling seamless communication between all the boards within the ATCA shelf through the Base Interface.

### 5.2.1 Components and functionality

Figure 5.5 presents a block diagram of the proposed design, which incorporates all the necessary components, detailed in the following subsection, to ensure full functionality. Additionally, a USB hub has been integrated into the design to enhance connectivity, particularly during debugging phases when multiple JTAG programmers may be required for programming the CPM.

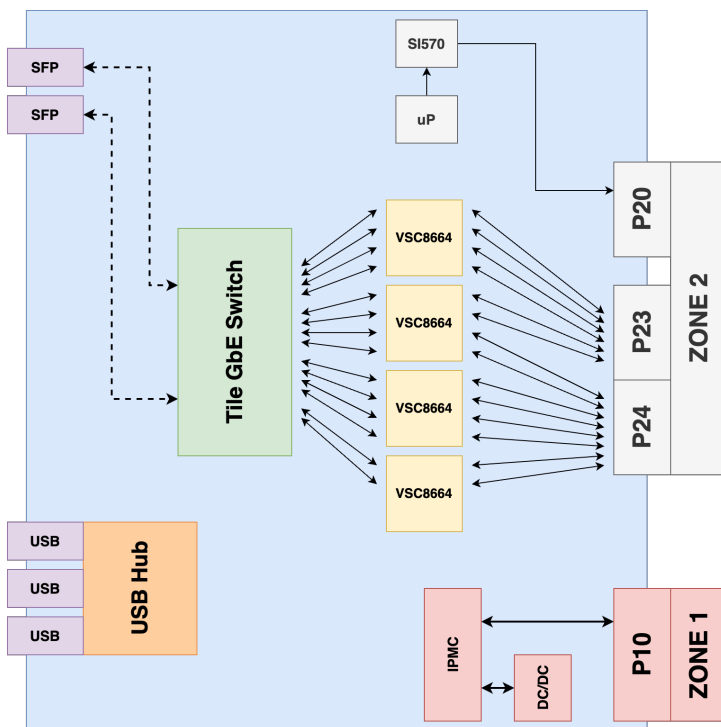


Figure 5.5: Simplified block diagram of the ATCA switch board design.

## Network

This design uses the 16-port GbE switch introduced in Chapter 2. The selection of this switch was driven by its proven reliability and capability to meet the system’s requirements, alongside its modular design, which facilitates future upgrades.

Two Small Form-factor Pluggable (SFP) ports are routed to the switch for front-panel communication. The choice of SFP over traditional RJ-45 connectors allows for greater flexibility in future system upgrades, avoiding limitations imposed by the Physical Layer (PHY) block.

The remaining ports of the GbE switch are connected to the Microchip VSC8664 [107]. The Microchip VSC8664 is a quad-port Gigabit Ethernet transceiver designed for applications requiring robust and efficient communication over Ethernet. It serves as a MAC-to-PHY converter, bridging the Media Access Control (MAC) layer with the PHY layer, supporting both 1000BASE-T and 100BASE-TX standards.

It includes advanced power management, auto-negotiation capabilities, and support for IEEE 802.3 standards. In the context of the ATCA switch board, it facilitates seamless connectivity between the Zone 2 Base Interface back-plane and the onboard Gigabit Ethernet switch.

Clock signals needed for the VSC8664 are generated from a 125 MHz clock connected to a low skew, low additive jitter single input to four output clock buffer device, a Diodes Incorporated PI6C39X020401 [108].

To ensure long-term adaptability, the Fabric Interface lines have been routed to unused ports on the GbE switch, allowing for potential future upgrades requiring speeds of up to 10 Gbps. Although this was not the initial design choice, using the existing GbE switch was preferred to maintain a modular architecture. This approach avoids integrating a fixed embedded switch controller, which would have constrained the system to a specific speed and limited future flexibility. Figure 5.6 presents a block diagram illustrating the complete network architecture of the system.

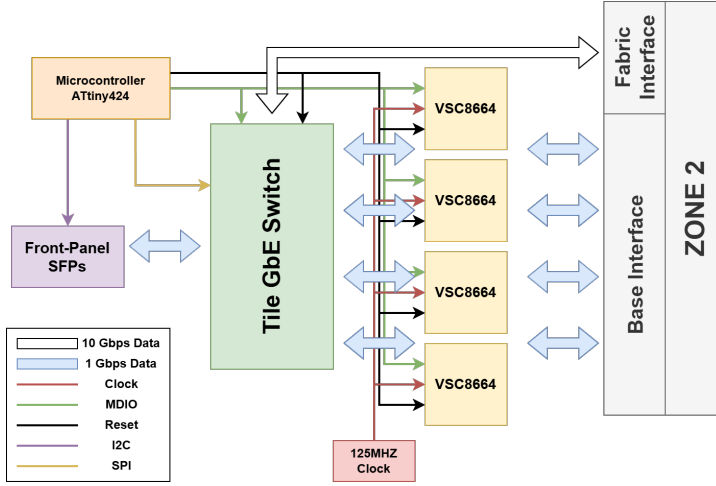


Figure 5.6: Detailed block diagram of the ATCA switch board network block design.

An Microchip ATtiny424-SS [109] micro-controller has been incorporated into the design to enable additional functionalities, such as I2C communication with the SFP modules, SPI communication with the GbE switch, and Management Data Input/Output (MDIO) access for configuration. It also provides reset control for the GbE switch and all VSC8664 components. While not strictly essential, the ATtiny424-SS microcontroller gives the possibility to enable dynamic configuration of the switch and PHY converters. It offers the option to implement default settings, allowing the board to function in a plug-and-play manner.

### Universal Serial Bus

When utilizing an ATCA crate for debugging operations, accessing USB devices can sometimes be challenging, particularly depending on the server's location. To streamline these debugging tasks, a USB hub has been integrated into the design. This allows a connection from the server to the hub, providing access to six USB-A ports.

For this implementation, the Texas Instruments TUSB2077A [110], a 7-

port Full-Speed (12 Megabits per second (Mbps)) USB 2.0 hub, was chosen as it meets the required specifications. The USB signals are routed to three dual USB connectors.

### Power Distribution and Management

The power distribution and management strategy incorporates several components to ensure reliable operation under varying loads, efficient power distribution, and monitoring capabilities. The components selected for the power distribution are the OmniOn Power QBDW033A0B41Z DC-DC converter [111], the OmniOn Power PIM400KZ Power Input Module [112], and an slot for the IPMC connection. Figure 5.7 shows a block diagram of the power system.

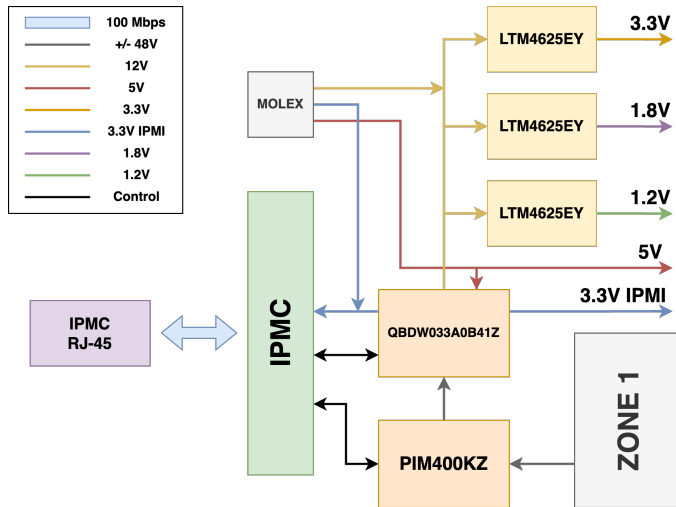


Figure 5.7: Detailed block diagram of the ATCA switch board power block design.

The QBDW033A0B41Z is a high-performance, isolated DC-DC converter specifically designed for ATCA environments. It provides a highly efficient conversion from the ATCA backplane's 48V input to a stable 12V output, which serves as the primary power source for the modules within the shelf.

The PIM400KZ functions as the interface between the shelf's power entry

module and the individual boards. It ensures stable power delivery, allows the insertion and removal of boards without disrupting the operation of other components (hot-swap support), real-time monitoring of power usage and supports fault detection. The PIM400KZ also provides 5V output for the USB hub and 3.3V output for the IPMC.

The IPMC, already mentioned in Chapter 2, controls the startup sequence of the QBDW033A0B41Z DC-DC converter and other power rails to ensure proper initialization of components, tracks the operating conditions, including voltage, current, and temperature, of all power distribution components, interfaces with the ATCA Shelf Manager over the IPMB for real-time status reporting and remote control and detects anomalies such as over-current or temperature excursions and takes corrective actions, including shutting down affected components or reporting issues to the system operator. An external dedicated RJ-45 connector has been added to the PCB design, providing access to the IPMCs Ethernet interface for debugging purposes.

To support the operation of various components within the ATCA switch board, the design incorporates three additional DC-DC converters based on the Analog Devices LTM4625EY [113]. These converters provide stable voltage outputs of 3.3 V, 1.8 V, and 1.2 V and a maximum current output of 5 A.

For enhanced versatility, a Molex 2x2 connector is included in the design. This connector facilitates debugging and testing activities outside the ATCA shelf environment, allowing to power and evaluate the board independently from the ATCA system.

## 5.3 Printed Circuit Board layout

The ATCA switch board is designed in compliance with the ATCA form factor, adhering strictly to the specifications outlined in the ATCA standard [103]. These standards define the physical and mechanical dimensions of the board, including constraints on the maximum allowable component height and the

precise placement of connectors. This ensures seamless integration within the ATCA shelf while maintaining compatibility with other ATCA-compliant modules and systems.

### 5.3.1 Stack-up

The selected PCB stack-up consists of 10 layers, designed to implement the power rails and signal routing effectively. Figure 5.8 illustrates the stack-up, highlighting the layer thickness and materials utilized.

The selected core material, FR4 (Tg-150), was chosen over alternatives to its adequacy for the operating speeds of this board, which are not critical. With a dielectric constant ( $\epsilon_r$ ) of 4.5, FR4 meets the design requirements, offering a cost-effective and reliable solution without the need for higher-performance materials typically used for high-speed applications [114]. The selected prepreg material is 2116, featuring 55% resin content and a  $\epsilon_r$  of 4.4.

The final layer distribution for the ATCA switch board PCB design is as follows:

- Layers 2, 3, 7, and 9 are designated as Ground (GND) planes.
- Layers 5 and 6 serve as split power planes.
- Layers 1, 4, 8, and 10 are allocated for signal routing.

The stack-up was designed to ensure that every signal or power layer is followed by a continuous ground plane, providing a consistent reference to ground. This approach enhances signal integrity and helps minimize noise throughout the PCB [115].

### 5.3.2 Design, Placement and Routing

For the schematic and PCB design, various software options were considered, but KiCAD was ultimately chosen due to its user-friendly interface and open-source nature. Its availability across multiple platforms further contributed to its selection, ensuring easy access and widespread usability.

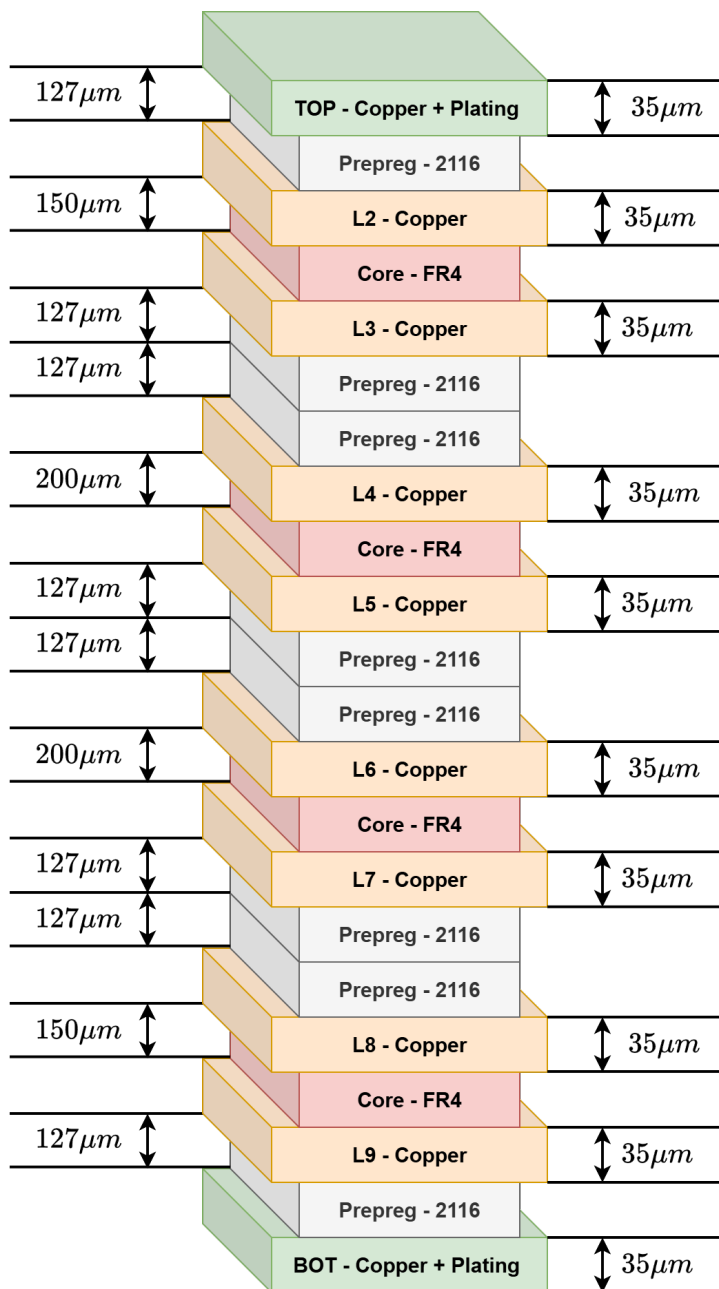


Figure 5.8: Sketch of the stack-up selected.



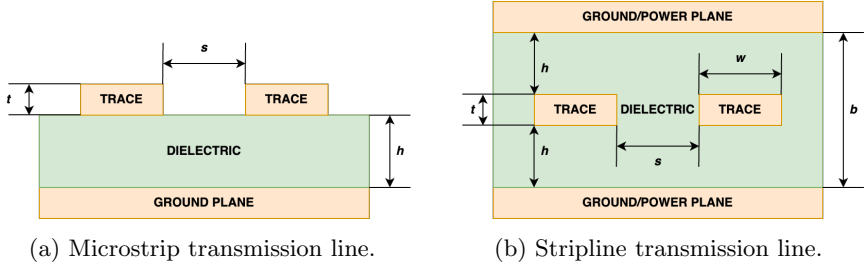


Figure 5.9: Cross-sectional views of microstrip (left) and stripline (right) transmission lines, illustrating the placement of traces, dielectric layers, and ground/power planes.

The PCB dimensions and layout were determined based on the ATCA standard [103]. In compliance with this standard, alignment pins, mounting holes, connectors, and other specified requirements were incorporated into the design to ensure full compatibility with the ATCA infrastructure.

Regarding the placement of the components, careful consideration was given to optimize functionality and ease of access. The power components were located close to the Zone 1 connector to minimize routing complexity and ensure efficient power delivery.

The PHY converters (VSC8664) were positioned near the Zone 2 connector to simplify the routing of necessary lines. The GbE switch was placed as close as possible to the VSC8664 converters while maintaining accessibility and ease of removal. Status LEDs were arranged at the top of the board in a clear and organized manner to provide an intuitive visual reference for debugging, enabling quick identification of the status of each channel.

SFP connectors were positioned at the upper portion of the front panel for convenient access. The USB hub was located at the bottom of the PCB. Other interfaces required for debugging purposes were positioned on the front panel to ensure easy accessibility and convenience during testing and troubleshooting.

Differential signals are required for routing network and USB connections, with characteristic impedances of 100 ohms and 90 ohms, respectively. Impedance calculations for these lines were performed applying simplified for-

mulas [116] to determine the impedance of microstrip (Equation 5.1) and stripline (Equation 5.2) configurations:

$$Z_{0-Microstrip}(\Omega) \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) \quad (5.1)$$

where  $h$  is the height above the ground plane,  $w$  is the trace width,  $t$  is the thickness of the line and  $\varepsilon_r$  is the dielectric material relative permittivity.

$$Z_{0-Stripline}(\Omega) \approx \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{1.9b}{0.8w + t} \right) \quad (5.2)$$

where  $b$  is the is the separation between ground planes,  $w$  is the trace width,  $t$  is the thickness of the line and  $\varepsilon_r$  is the dielectric material relative permittivity.

Also, from [117], we can obtain that:

$$Z_{Diff-Microstrip}(\Omega) \approx 2Z_{0-Microstrip} \left( 1 - 0.48 \exp^{-0.96 \frac{s}{h}} \right) \quad (5.3)$$

where  $s$  is the is the separation tracks and  $h$  is the height of the traces above the reference plane.

$$Z_{Diff-Stripline}(\Omega) \approx 2Z_{0-Stripline} \left( 1 - 0.78 \exp^{-2.9 \frac{s}{h}} \right) \quad (5.4)$$

where  $s$  is the is the separation tracks and  $h$  is the distance between the planes.

The calculated width and separation values for the USB and GbE differential pairs are summarized in Table 5.1. These values fall within 10% of the target impedance specifications. To ensure accuracy, all impedance calculations were validated using KiCAD's integrated PCB trace impedance calculator.

|                                   |                   | Width        | Separation   |
|-----------------------------------|-------------------|--------------|--------------|
| <b>GbE Pair</b> ( $100\ \Omega$ ) | <b>Microstrip</b> | $125\ \mu m$ | $140\ \mu m$ |
|                                   | <b>Stripline</b>  | $125\ \mu m$ | $160\ \mu m$ |
| <b>USB Pair</b> ( $90\ \Omega$ )  | <b>Microstrip</b> | $150\ \mu m$ | $180\ \mu m$ |
|                                   | <b>Stripline</b>  | $150\ \mu m$ | $210\ \mu m$ |

Table 5.1: Summary of the chosen geometric parameters for the high-speed interconnects.

## 5.4 Verification and Performance

After the board was manufactured, a Time Domain Reflectometry (TDR) measurement was performed using a Keysight DCA-X 86400D oscilloscope with the Keysight 54754A Differential TDR module to characterize the longest traces associated with the GbE links. TDR is a widely used technique for evaluating the quality of high-speed interconnects. It involves sending a step signal with a fast rise time through the trace and observing the amplitude of the reflected signal in the time domain. Variations in impedance along the line cause changes in the reflected signal, with discontinuities resulting in either increased or decreased amplitudes depending on the nature of the mismatch.

Figure 5.10 shows the TDR result for one of the longest PCB traces used for the GbE lanes. The initial portion of the trace corresponds to the probe itself, while the disturbance observed in the middle indicates the transition from the probe to the PCB trace. The impedance along the entire trace is visible, located around 80 ohm, shows a deviation from the expected 100 ohm value.

This discrepancy may be attributed to the fact that the board was manufactured without impedance control, a choice made to reduce production costs. Nonetheless, even with impedance-controlled fabrication, manufacturers typically guarantee tolerances only within 10% of the target impedance. A different type of dielectric material would also improve this result. However, this discrepancy does not affect the proper functioning of the design, as will be demonstrated later.

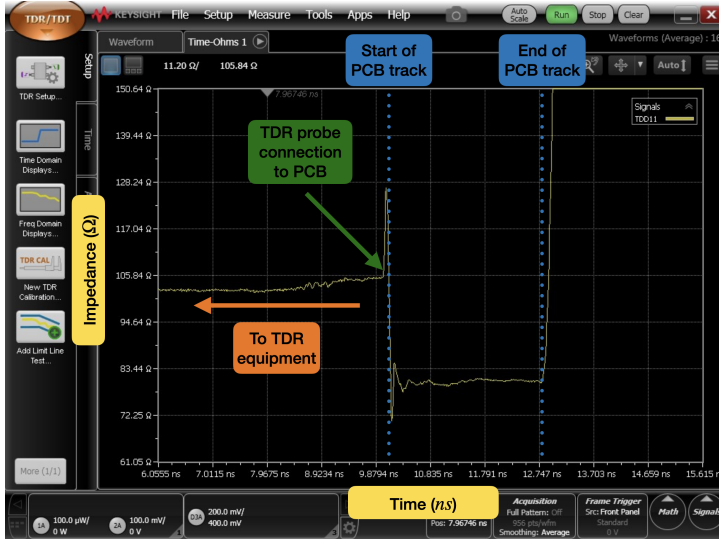


Figure 5.10: Screenshot of the TDR measurement performed to one of the longest PCB traces associated with the GbE lanes.

Once the board was fully assembled (Figure 5.11), a comprehensive inspection was conducted to verify its electrical integrity and functionality. The board was thoroughly tested for potential shorts, and all voltage and current measurements were found to be within the expected ranges. The USB hub was also validated, confirming it worked correctly without any issues.

For testing the communication functionality, a dedicated test setup was developed. Ideally, the ATCA switch board would be connected to one of the hub slots in the ATCA shelf (Slot 1 or 2), while the ACBB board would occupy one of the remaining slots. However, at the time of writing this thesis, the TileCoM—responsible for communicating with the switch—is not yet available in its final hardware version, which will resolve the power distribution issues described in Chapter 4.

To overcome this limitation and evaluate the system’s performance, a second ATCA switch board was used in place of the carrier board. Figure 5.12 presents a block diagram of the test configuration, while Figure 5.13 shows the real setup implemented in the lab. The configuration consists of a private

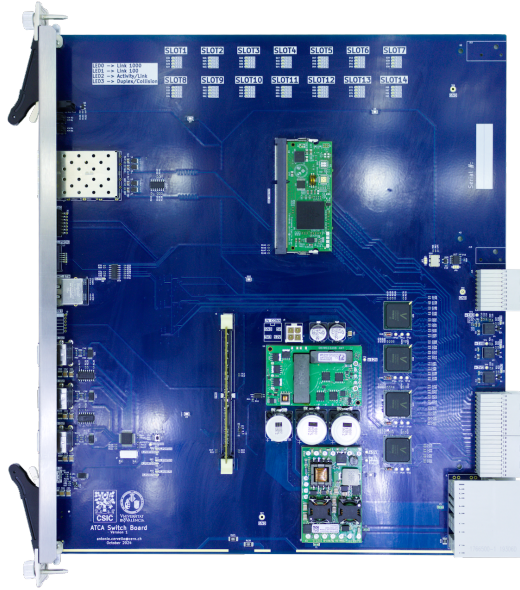


Figure 5.11: ATCA switch board fully assembled.

network created on a server *Server 1*, which is connected to the ATCA switch board placed in Slot 2 (a hub slot). Communication through the ATCA shelf's Zone 2 backplane reaches Slot 8, where the second ATCA switch board is installed. A second server, *Server 2*, is connected to this board to complete the testing environment.

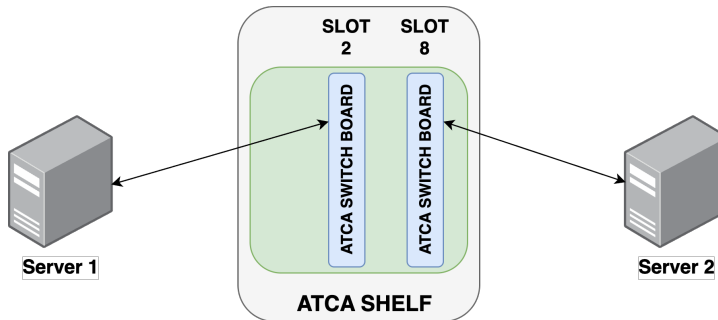


Figure 5.12: Block diagram of the performance test setup for the ATCA Switch board.



Figure 5.13: Picture photograph of the performance test setup conducted at the Valencia laboratory.

The performance evaluation was carried out using the *iperf3* utility, a network testing tool used to measure the maximum achievable bandwidth between two endpoints over an IP network. A 100-second bidirectional test was initially conducted, confirming that the ATCA switch board could reach data transfer speeds close to the intended 1 Gbps design target. No transmission errors were detected during the test, demonstrating stable and reliable communication. The test results are presented in Figure 5.14. Additionally, extended long-duration tests lasting several hours were performed to further verify the consistent and correct behavior of the system under sustained load.

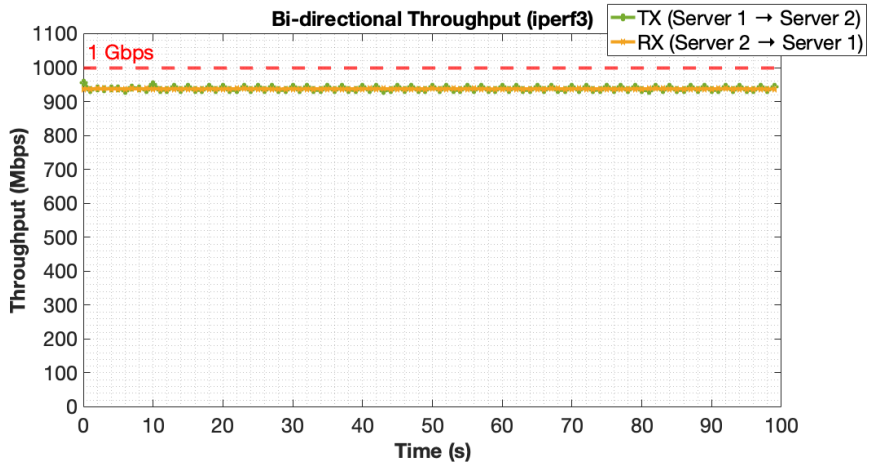


Figure 5.14: Results of the performance test using the *iperf3* tool, showing simultaneous transmission and reception. The plot demonstrates that the system achieves throughput close to the designed 1 Gbps target.





## Chapter 6

# Testbeam setup and results

*This chapter presents a summary of the testbeam campaigns carried out at the H8 beam line at CERN to validate the upgraded TileCal systems for Phase-II. A comprehensive description of the testbeam setup, facilities, trigger and readout architecture is provided, along with an overview of the physics measurements and calibration results obtained, demonstrating the readiness of the new infrastructure for integration into ATLAS.*

Several testbeam campaigns were carried out at the H8 beam line of the CERN SPS accelerator in the Preveessin area during 2015 and 2024. Typically, each testbeam period spans 14 days of beam time, allowing for a comprehensive series of measurements [118]. During these campaigns, modules were tested using beams of varying energies and different particles, both along the  $\eta$  direction and in perpendicular positions relative to the beam.

## 6.1 Introduction

The primary motivations of the testbeam campaigns are to evaluate the stability of the readout electronics and to validate the trigger and readout architectures planned for the Phase-II upgrade as well as to verify and optimize the measurement of the electromagnetic energy scale.

Until June 2024, the TilePPr demonstrator prototype was installed in the H8 control room, where it was used to read out and operate the upgraded modules and to transfer selected data to the legacy RODs and FELIX system. However, starting in September 2024, the TilePPr demonstrator was replaced by the final design of the CPM, enabling testing of the complete final data path, including integration with FELIX.

## 6.2 Testbeam setup

The calorimeter setup was positioned at the H8 beam line in CERN's SPS North Area. It consisted of five TileCal modules placed on a scanning table capable of adjusting both the angle and position relative to the incident beam. Two Long Barrel modules (LBA02 and LBC01) were instrumented with the legacy readout electronics described in Chapter 1. A third Long Barrel module (LBA01) was also equipped with legacy electronics but included a modified configuration that featured a Multi-Anode Photomultiplier Tube (MAPMT), providing the potential to enhance the calorimeter's spatial resolution [119]. The MAPMT was used for future studies unrelated to the Phase-II upgrade. These three modules contained PMT blocks with 3-in-1 cards, Digitizer boards, and Interface boards to facilitate communication with the back-end electronics. The legacy modules were essential during the testbeams, allowing for direct comparisons between the legacy and upgraded readout electronics.

Regarding the upgrade modules, one Long Barrel (LBC02) and one Extended Barrel (EBC03) upgraded modules were equipped with four and three mini-drawers, respectively, each connected to a cooling system to regulate in-

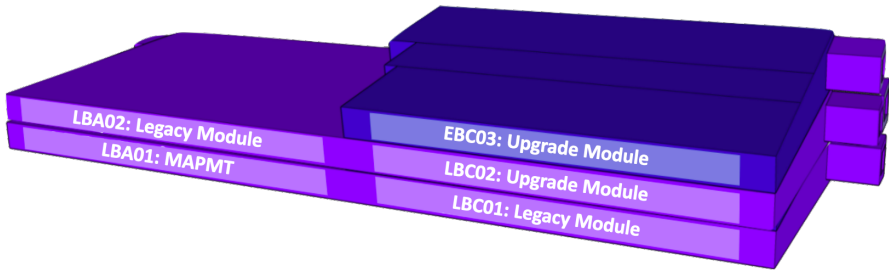


Figure 6.1: Configuration of the modules in the Tile Calorimeter testbeam setup since 2022.

ternal temperatures. Each mini-drawer housed one DaughterBoard, one MainBoard, and 12 PMT blocks with the upgraded front-end boards, the FENICS cards. The LBC02 module was specifically outfitted with 45 PMTs utilizing FENICS cards, along with four MainBoards v4 and four DaughterBoards v6.4. Similarly, the EBC03 module was equipped with 32 PMTs, also using FENICS cards, four MainBoards v4, and four DaughterBoards v6.4. Figure 6.1 and Figure 6.2 shows the configuration and positioning of the modules during the testbeam periods.

Regarding the services, HV was supplied to each PMT from the H8 control room. The upgraded modules received LV power from an LVBox attached to the end of the module, which was controlled via Controller Area Network Bus (CANBus) through the DCS software.

The back-end electronics combined both legacy and upgraded systems. The legacy electronics included a reduced version of the original back-end system, consisting of one ROD, two SBC (one for the ROD crate and one for the TTC carte), and one TBM. The upgraded modules transmitted data to two TilePPr Demonstrators, which were integrated with the legacy TDAQ software via TTC and ROD interfaces. The TilePPr Demonstrator (Figure 6.3) was specifically designed to evaluate the performance of the upgraded electronics and trigger interfaces in preparation for the HL-LHC. The TilePPr Demonstrator is capable of operating and reading out one TileCal module [120], therefore



Figure 6.2: Picture of the TileCal testbeam modules on the table.

two TilePPr Demonstrator were needed. The TilePPr Demonstrators also sent data in parallel to the FELIX system, using a FLX-712 card running the latest GBT mode Phase-II firmware at the time. During the September 2024 test-beam campaign, the TilePPr Demonstrators were replaced by a CPM, capable of reading up to two TileCal modules, marking the integration of the final data path. A TTC system, composed of an ALTI system, was also present in the testbeam setup. This system was used to configure both the upgraded and legacy electronics via TDAQ software, as well as to provide the clock signal for the readout electronics.

### 6.2.1 Beam elements

Various detectors were installed along the beam line to monitor the beam's quality, position, and particle composition. Figure 6.4 provides a diagram of the beam elements used in the testbeam setup.

Two Delay Wire Chamber (DWC) were employed to measure the beam position with a resolution of 0.2 mm, aiding in determining the beam's impact point on the TileCal modules. Developed at CERN, the DWC consists of two "*sandwich*" parts, each composed of two cathode planes surrounding a

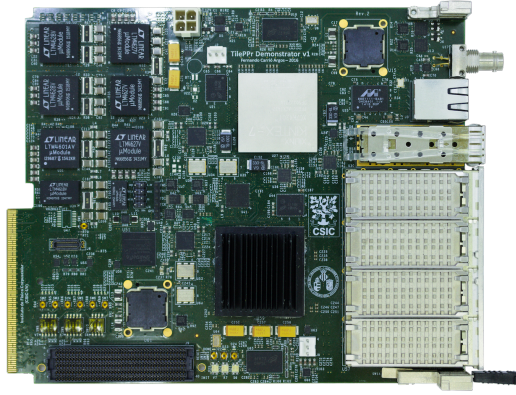


Figure 6.3: TilePPr Demonstrator module readout system.

central anode wire plane. These parts are positioned orthogonally to each other, allowing for two-dimensional position measurements.

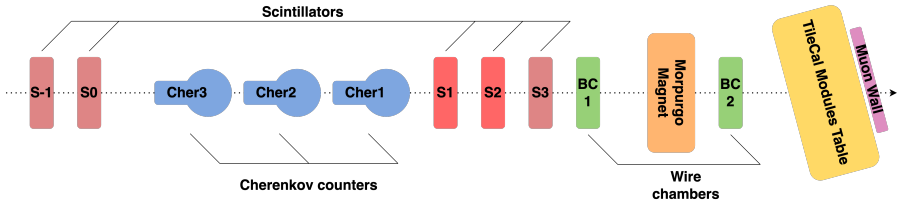


Figure 6.4: Beam elements schema of the testbeam setup. Dashed line represents the beam trajectory.

Since the beam was not composed of a single type of particle, a Muon Hodoscope (MH) and three Cherenkov Counters (CC) were included to assist in offline data analysis by providing additional particle identification information. The MH, also referred to as the Muon Wall, is a movable detector consisting of 12 scintillators positioned behind the Tile modules. It is primarily used in offline analysis to suppress the low-energy tail of pions during high-energy hadron runs [121]. The CC were placed in the beam line to improve particle identification by distinguishing protons, pions, electrons, and kaons.

Two scintillators, S1 and S2, were also installed in the beam line as part of the beam trigger system. Their signals were transmitted to the control room's

122

## 6.3 Data acquisition

The front-end electronics transmit data to the TilePPr, which processes it into two distinct paths. The first path emulates the legacy system by formatting the data with 7 samples at 10 bits per sample. For the testbeam campaign, the legacy ROD system was modified in order to accept 15 samples. This data is then packed for transmission via G-Link, the format compatible with the legacy ROD inputs.

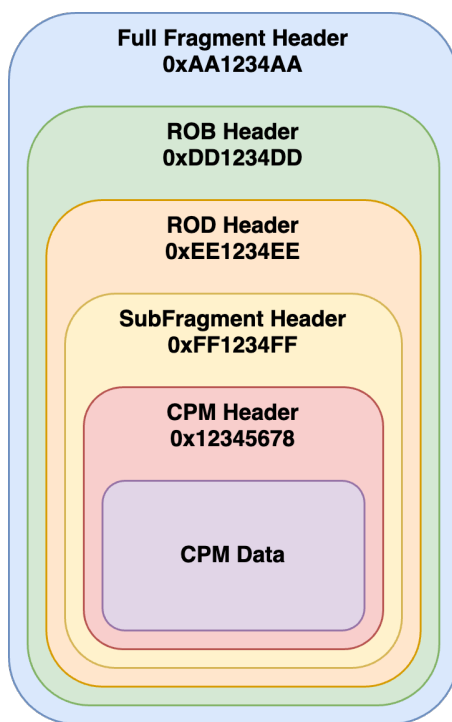


Figure 6.6: Complete data packet structure following the ATLAS Event Format for the Tile upgrade electronics, including the subfragment header to ensure compatibility with the legacy readout system during testbeam campaigns.

Simultaneously, the TilePPr processes the data into the FELIX format, utilizing 16 samples at 12 bits per sample, including both HG and LG signals. This data packet is transmitted to the FELIX system, which redistributes

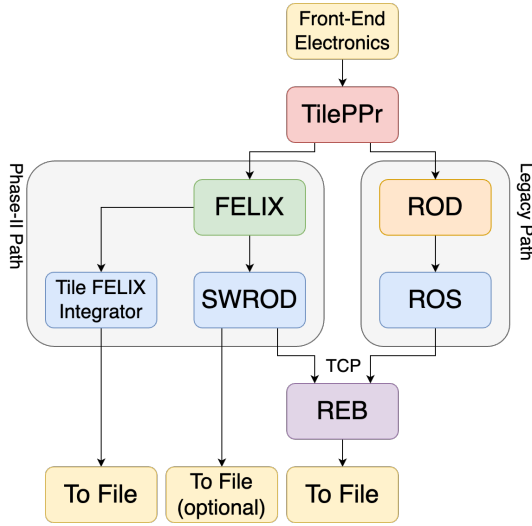


Figure 6.7: Data acquisition scheme of the testbeam setup.

it to the SWROD system. Within the SWROD, the software validates the packet’s integrity by cross-verifying the L1ID and BCID in the data packet against those provided by FELIX, ensuring synchronization. Furthermore, to ensure compatibility with the REB system, additional information must be included in the data packet. Specifically, a subfragment header —previously used in the legacy system— must be appended to the packet to meet the REB format requirements (Figure 6.6). Once verified, the packet is forwarded to the fragment consumer, as detailed in Chapter 3. There, it is encapsulated into the ATLAS event format to merge with the legacy data packet in the REB block via TCP. The REB then combines all data into a raw data file for offline reconstruction.

Additionally, integrator data is collected independently without disrupting fast-readout operations. This is accomplished using the Tile FELIX integrator readout software, which saves the integrator data into files for offline reconstruction, as discussed in Chapter 3.

Figure 6.7 illustrates the data acquisition architecture in the test beam area for the Tile Calorimeter.



## 6.4 Data Quality Monitoring

During data acquisition, DQM application (see Figure 6.8) was employed to verify and ensure the quality of the data being collected in real time. Additionally, the DQM provided information about beam line elements, aiding in the identification and resolution of issues during data taking. This functionality relied on specific segments within the TDAQ partition, namely the Tile Stateless Monitoring and Tile Gatherer segments. These segments sampled events from the REB, processed them to generate diagnostic plots, and published these plots to the TDAQ online histogramming software. The DQM application subsequently queried these plots and displayed them in organized blocks. The DQM employed a semaphore-style color-coding system, enabling users to rapidly identify potential issues.

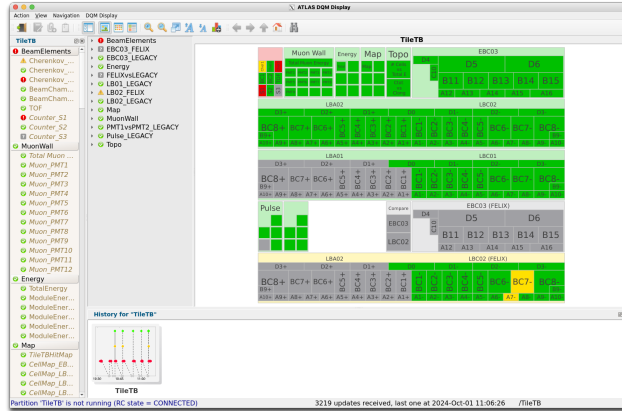


Figure 6.8: Data Quality Monitoring panel at the testbeam area during September 2024 testbeam campaign.

For debugging purposes, the *EventViewer* tool [122] was also utilized. This software allowed on-the-fly selection and inspection of individual events, providing access to their raw data. To decode TileCal packets, the *TileEventViewer* plugin was used, facilitating the parsing and interpretation of event data. This plugin was updated to support the new data packets introduced by the FELIX system. Figure 6.9 presents examples of FELIX packets

decoded during the latest testbeam campaign.

| Register Name  | MiniDrawer 1 | MiniDrawer 2 | MiniDrawer 3 | MiniDrawer 4 |
|----------------|--------------|--------------|--------------|--------------|
| SWROD Status   | 0            | 0            | 0            | 0            |
| FELIX Status   | 0            | 0            | 0            | 0            |
| Module ID      | 0x065        | 0x065        | 0x065        | 0x065        |
| Packet Version | 1            | 1            | 1            | 1            |
| Fragment Size  | 2            | 2            | 2            | 2            |
| Pedestal HG    | 566          | 566          | 566          | 566          |
| Pedestal LG    | 2146         | 2146         | 2146         | 2146         |
| CIS Cap        | 0            | 0            | 0            | 0            |
| CIS Time       | 0            | 0            | 0            | 0            |
| CIS Charge     | 512          | 512          | 512          | 512          |
| MD ID [0..3]   | 0            | 1            | 2            | 3            |
| BCID           | 0x637        | 0x637        | 0x637        | 0x637        |
| xL1ID          | 0x00005eec   | 0x00005eec   | 0x00005eec   | 0x00005eec   |
| BCR counter    | 0x02a5c538   | 0x02a5c538   | 0x02a5c538   | 0x02a5c538   |

| Cell  | PMT | Ch | G | Smp0 | Smp1 | Smp2 | Smp3 | Smp4 | Smp5 | Smp6 | Smp7 | Smp8 | Smp9 | Smp10 | Smp11 | Smp12 | Smp13 | Smp14 | Smp15 |
|-------|-----|----|---|------|------|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|
| D0    | 01  | 00 | 1 | 135  | 133  | 131  | 132  | 133  | 130  | 131  | 134  | 129  | 130  | 132   | 134   | 132   | 137   | 130   | 130   |
| A1-L  | 02  | 01 | 1 | 138  | 143  | 139  | 137  | 144  | 141  | 144  | 135  | 144  | 138  | 141   | 138   | 138   | 142   | 139   | 142   |
| BC1-R | 03  | 02 | 1 | 136  | 136  | 136  | 139  | 135  | 142  | 133  | 135  | 131  | 135  | 136   | 137   | 134   | 137   | 134   | 135   |
| BC1-L | 04  | 03 | 1 | 145  | 144  | 142  | 148  | 142  | 145  | 145  | 147  | 150  | 148  | 148   | 140   | 142   | 145   | 142   | 141   |
| A1-R  | 05  | 04 | 1 | 144  | 146  | 149  | 143  | 143  | 146  | 146  | 144  | 145  | 141  | 144   | 144   | 143   | 148   | 143   | 144   |
| A2-L  | 06  | 05 | 1 | 167  | 169  | 172  | 171  | 170  | 172  | 169  | 168  | 171  | 171  | 170   | 173   | 169   | 171   | 173   | 174   |
| BC2-R | 07  | 06 | 1 | 155  | 157  | 154  | 157  | 158  | 159  | 151  | 159  | 158  | 150  | 154   | 155   | 155   | 156   | 154   | 154   |
| BC2-L | 08  | 07 | 1 | 146  | 150  | 144  | 141  | 143  | 145  | 147  | 144  | 148  | 146  | 149   | 149   | 146   | 142   | 145   | 145   |
| A2-R  | 09  | 08 | 1 | 137  | 128  | 132  | 135  | 128  | 133  | 131  | 134  | 133  | 137  | 134   | 133   | 130   | 133   | 131   | 136   |
| A3-L  | 10  | 09 | 1 | 135  | 137  | 136  | 130  | 141  | 135  | 137  | 137  | 141  | 134  | 133   | 136   | 132   | 136   | 136   | 138   |
| A3-R  | 11  | 10 | 1 | 154  | 154  | 148  | 151  | 148  | 150  | 153  | 150  | 154  | 147  | 153   | 155   | 154   | 153   | 151   | 151   |
| BC3-L | 12  | 11 | 1 | 160  | 153  | 157  | 155  | 149  | 161  | 152  | 156  | 155  | 157  | 157   | 154   | 157   | 153   | 156   | 158   |

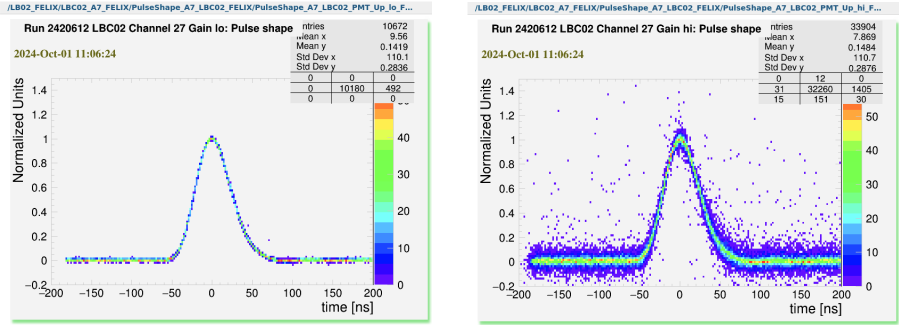
| Cell  | PMT | Ch | G | Smp0 | Smp1 | Smp2 | Smp3 | Smp4 | Smp5 | Smp6 | Smp7 | Smp8 | Smp9 | Smp10 | Smp11 | Smp12 | Smp13 | Smp14 | Smp15 |
|-------|-----|----|---|------|------|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|
| D0    | 01  | 00 | 0 | 124  | 124  | 124  | 126  | 125  | 126  | 125  | 124  | 127  | 126  | 124   | 125   | 126   | 125   | 126   | 125   |
| A1-L  | 02  | 01 | 0 | 149  | 152  | 149  | 149  | 148  | 151  | 148  | 149  | 148  | 148  | 151   | 149   | 151   | 149   | 150   | 151   |
| BC1-R | 03  | 02 | 0 | 113  | 114  | 115  | 116  | 115  | 113  | 114  | 115  | 115  | 114  | 113   | 115   | 113   | 114   | 113   | 115   |
| BC1-L | 04  | 03 | 0 | 141  | 138  | 140  | 140  | 139  | 136  | 140  | 140  | 138  | 138  | 140   | 139   | 140   | 140   | 142   | 138   |
| A1-R  | 05  | 04 | 0 | 148  | 148  | 147  | 148  | 149  | 146  | 147  | 148  | 146  | 148  | 147   | 148   | 148   | 148   | 148   | 149   |
| A2-L  | 06  | 05 | 0 | 147  | 147  | 147  | 147  | 146  | 146  | 148  | 147  | 145  | 149  | 147   | 147   | 147   | 145   | 146   | 148   |
| BC2-R | 07  | 06 | 0 | 145  | 147  | 146  | 146  | 145  | 148  | 144  | 146  | 146  | 145  | 147   | 147   | 146   | 145   | 145   | 146   |
| BC2-L | 08  | 07 | 0 | 155  | 154  | 155  | 156  | 157  | 155  | 156  | 155  | 156  | 157  | 155   | 155   | 156   | 156   | 156   | 158   |
| A2-R  | 09  | 08 | 0 | 128  | 127  | 128  | 129  | 128  | 129  | 129  | 128  | 127  | 127  | 128   | 128   | 127   | 129   | 128   | 128   |
| A3-L  | 10  | 09 | 0 | 117  | 118  | 119  | 117  | 120  | 118  | 118  | 117  | 117  | 118  | 118   | 119   | 118   | 117   | 117   | 116   |
| A3-R  | 11  | 10 | 0 | 145  | 146  | 146  | 144  | 147  | 146  | 146  | 144  | 145  | 144  | 145   | 144   | 145   | 144   | 145   | 145   |
| BC3-L | 12  | 11 | 0 | 155  | 155  | 154  | 156  | 154  | 155  | 153  | 155  | 154  | 154  | 153   | 154   | 155   | 155   | 154   | 155   |

Figure 6.9: Screenshot of the *TileEventViewer* plugin displaying the decoding of a long barrel FELIX data packet, showcasing both HG and LG readings.

## 6.5 Results

Reliable data acquisition has been achieved during the last testbeam campaigns, enabling the seamless combination of legacy and upgraded data into a unified file format to facilitate reconstruction and comparison. Figures 6.10a and 6.10b illustrate LG and HG pulses from the FELIX readout, respectively. The system's functionality has been fully validated using both legacy and upgraded readout paths.

Comparisons were performed during calibration and physics runs to evaluate the consistency between the legacy and FELIX readout systems. The results, as depicted in Figure 6.11, show no significant discrepancies between the two, confirming their compatibility and accuracy. Legacy values are scaled by a factor of 4 to compensate for the bit-depth difference between the 12-bit



(a) Low Gain pulse shape.

(b) High Gain pulse shape.

Figure 6.10: Pulse shape coming from the A7 cell during Run 2420612 taken during the testbeam campaign in September 2024 using the FELIX and SWROD system.

data used in the FELIX system and the 10-bit format of the legacy readout. This adjustment is necessary because the TilePPr discards the two most significant bits from the 12-bit data when transmitting it to the legacy ROD system.

To validate the functionality of the Tile Integrator software, several Cesium calibration runs were performed. After reconstructing the data acquired with the Tile FELIX integrator software, the results—shown in Figure 6.12—confirm the correct operation of the readout and successful data reconstruction.

To further assess the performance of the upgraded readout system, a noise correlation analysis was performed comparing it with the legacy system. Bi-dimensional noise correlation plots were generated, where each axis represents the 48 readout channels of a module, and the color scale indicates the level of correlation between their amplitudes. High levels of correlation suggest the presence of coherent noise sources affecting multiple channels simultaneously.

Figure 6.13 presents a comparison between the legacy module (LBC01) through the legacy readout and the upgrade module (LBC02) equipped with the FELIX readout, both tested during the same testbeam campaign. The legacy system displays strong correlations across many channels, indicative of shared noise contributions. In contrast, the upgraded FELIX-based system

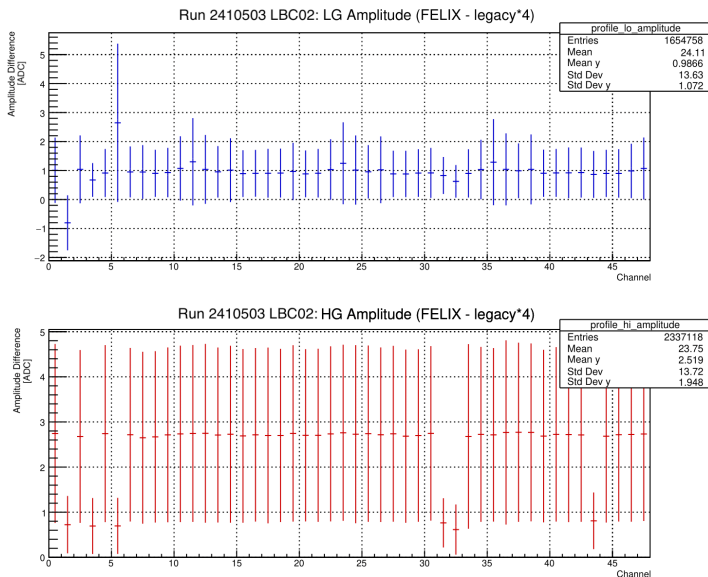


Figure 6.11: Comparison of low-gain (top) and high-gain (bottom) amplitude differences between FELIX and legacy readouts during a pedestal run (Run Number 2410503) in the upgrade module. Lower values indicate uninstrumented or noisy channels.

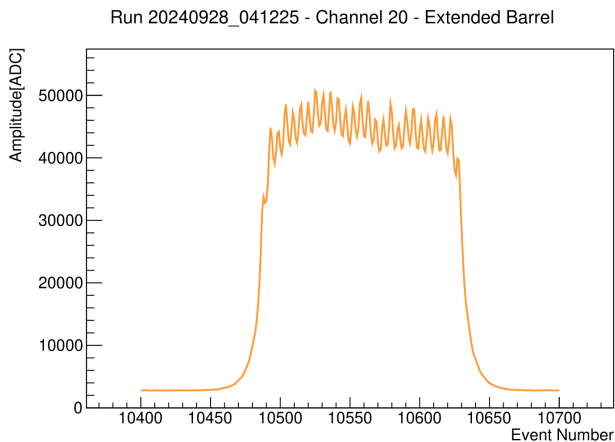


Figure 6.12: Plot of the integrator readout obtained via FELIX, displaying the ADC counts measured as the Cesium capsule passes through channel 20 (Cell A14-R) of the extended barrel during September 2024 testbeam campaign.

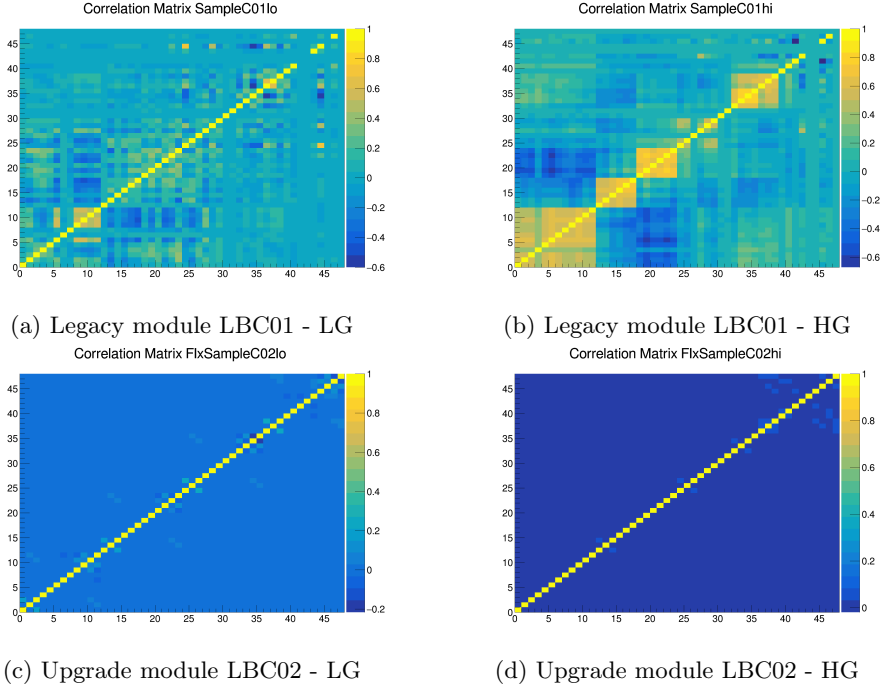


Figure 6.13: Noise correlation comparison between a legacy module using the legacy readout and an upgraded module using the FELIX readout, obtained from a pedestal run (Run Number 2420799). Both axes represent the channel number of the module.

exhibits significantly reduced correlation, demonstrating a marked improvement in noise isolation and overall signal integrity of the new electronics. This result validates the effectiveness of the new electronics in mitigating coherent noise effects within the detector module.



## Chapter 7

# Implementations in ATLAS - Demonstrator

*This chapter focuses on the implementation and integration of the new readout path for the Demonstrator project within the ATLAS experiment. It covers the setup and configuration of the FELIX readout system, integration with TDAQ, and tests performed in both the Tile Standalone and ATLAS partitions. Lastly, it discusses the outcomes of these tests, including calibration data.*

### 7.1 Introduction

The Demonstrator project was designed to evaluate the proposed DAQ architecture and detector readout electronics for the HL-LHC before their integration into the ATLAS detector. A Demonstrator module, equipped with prototypes of all new components, was extensively tested during testbeam campaigns. This module consists of four mini-drawers, each capable of operating and reading out up to 48 PMTs. Each mini-drawer includes twelve 3-in-1 cards, one MainBoard, one DaughterBoard, and an HVbus board. For

the off-detector electronics, the readout was managed via the TilePPr Demonstrator.

In the back-end electronics, the TilePPr prototype manages the distribution of configuration commands and the sampling clock to the front-end electronics while receiving digitized data synchronized to the LHC clock. The DAQ architecture used for the Demonstrator aligns closely with the proposed HL-LHC system. However, the Demonstrator module still provides analog trigger signals to the L1Calo system, as it uses an upgraded 3-in-1 card (compatible with the existing setup) instead of the FENICS cards for the HL-LHC upgrade. This allows seamless integration with the current ATLAS detector trigger infrastructure.



Figure 7.1: Tile Demonstrator module in the ATLAS detector during maintenance activities.

Since its deployment in ATLAS, the Demonstrator module (Figure 7.1), introduced in the LBA14 module in July 2019 and fully integrated in May 2020, has continuously collected data using the legacy RODs as the main readout system, operating continuously throughout Run 3 data-taking. To ensure backward compatibility with the legacy system, the Demonstrator's data packets were adapted accordingly, following the same approach used during the testbeam campaigns described in Chapter 6. Figure 7.2 illustrates the readout configuration in use up to the Year-End Technical Stop (YETS) 2024.

During the YETS 2024/2025 period, the TilePPr Demonstrator was re-



placed with the CPM (Figure 7.3). With the integration of the CPM, the full data path exploiting the FELIX system was enabled, replicating the parallel readout setup demonstrated in the testbeam: data acquisition via both the legacy system and the FELIX system.

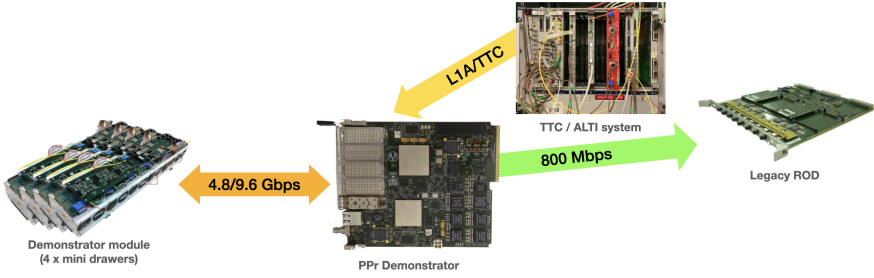


Figure 7.2: Tile Demonstrator module readout before YETS 2024.

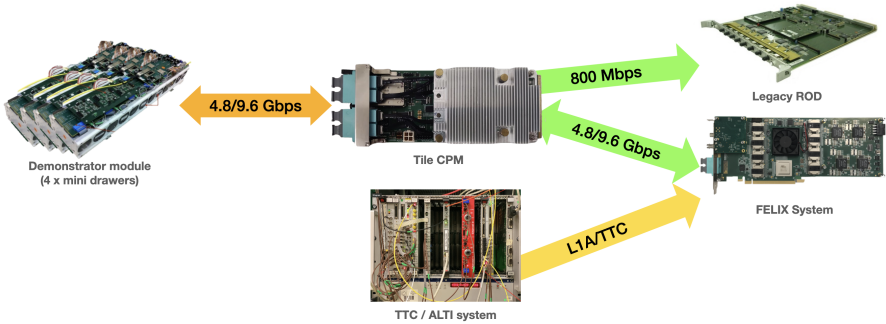


Figure 7.3: Tile Demonstrator module readout after YETS 2024.

## 7.2 Installation

The infrastructures required for the FELIX readout in the TilePPr system are installed in USA15. This includes electronics, data acquisition systems, power supplies, and cooling systems.

The FELIX and SWROD servers were installed in USA15 by the TDAQ



Figure 7.4: Photograph of the FELIX card used for the Tile Demonstrator readout. Visible connections include the MTP fiber (purple) for data transmission and clock distribution, and the ST fiber (orange) receiving the clock signal from the Tile LBA ALTI system.

team. TTC information is transmitted from the TTC LBA patch panel, located at Y.08-16.A1 (CERN internal location reference), to the Tile FELIX server at Y.05-05.A1 using an Straight Tip (ST)-ST OM2 fiber. For data transmission, a Multifiber Termination Push-on 24 (MTP24)-MTP24 OM4 fiber connects the FELIX server at Y.05-05.A1 (Figure 7.4) to a fiber cassette at Y.22-04.A1. This cassette converts the MTP24 fiber connection to 24 Lucent Connector (LC) connections, in order to make the FELIX-to-CPM connection in the TilePPr. The LC-LC fiber output from the cassette is then connected to the CPM in the TilePPr, located at Y.22-02.A1. A schematic of these connections is shown in Figure 7.5.

The FELIX cards have been configured to operate in GBT mode at 4.8 Gbps. Although the Phase-II upgrade will use FullMode (9.6 Gbps), the current configuration remains in GBT mode, as extensive tests conducted during test benches and testbeam campaigns have demonstrated its reliability and sta-

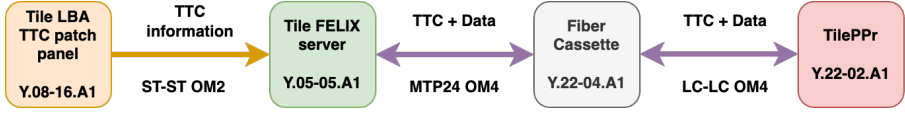


Figure 7.5: Diagram illustrating the fiber distribution at USA15 for the Tile FELIX readout in the Demonstrator setup.

ble performance. The configuration of the FELIX system is managed through the *Supervisord* application, ensuring seamless integration and operation. Additionally, the SWROD system has been integrated into the TDAQ framework, enabling it to capture and process all data transmitted by the FELIX system effectively.

## 7.3 Integration tests

To ensure seamless data capture, initial testing is conducted using the Tile Standalone partition. Once the system is thoroughly verified and validated, integration into the ATLAS partition can proceed.

### 7.3.1 Tile Standalone partition

The Tile Standalone partition serves as a platform for debugging, testing, and conducting calibration runs for the Tile Calorimeter. To accommodate the FELIX readout system, the partition was updated to include all necessary modifications, such as integrating the SWROD segment alongside the existing segments. This partition requires the same configuration used in the testbeam setup to enable data acquisition from FELIX and combine it into a unified raw data file with data from other modules. This functionality is made possible by a specialized fragment consumer, which transmits the SWROD data to the REB. At the REB, all fragments are merged into a single raw data file, as detailed in Chapter 3 and Chapter 6. The purpose of the tests in the Tile Standalone partition is to validate the correct operation of the system in a controlled test environment using the final data path layout, while ensuring compatibility with the legacy readout system for testing purposes.

### 7.3.2 ATLAS partition

The ATLAS partition operates slightly differently from the Tile Standalone partition. While both partitions use the same data path, the fragment consumer employed in SWROD to combine data into the REB is not required in the ATLAS partition, as the REB system is now deprecated and not used in ATLAS. Instead, data from the ROSES is sent directly to the HLT system, where it is subsequently combined into raw data files.

For the Tile Calorimeter’s FELIX system, the SWROD needs to be configured within the ATLAS partition’s Tile segment to route data to the HLT. Special consideration is necessary to distinguish data originating from the Demonstrator legacy path (via RODs) and the FELIX system, as both contain the same information but follow different routes. Maintaining both readouts serves several purposes: providing a backup system in case the FELIX readout encounters issues, enabling further comparisons between the legacy and FELIX systems, and leveraging the enhanced resolution and additional samples provided by FELIX.

Figure 7.6 presents a block diagram of the upgraded readout path implemented in ATLAS. The diagram illustrates the two output paths from the TilePPr: one directed toward the Phase-II readout system (FELIX and SWROD), and another that emulates the legacy system to enable parallel data acquisition. Both readout streams are transmitted to the HLT. The red block highlights a special path used exclusively during Tile Standalone operations, such as calibration procedures or standalone testing outside the ATLAS TDAQ partition.

## 7.4 Results

Due to ongoing data-taking campaigns, tests were limited to the Tile Standalone partition. The SWROD was correctly integrated and validated by acquiring data from several laser calibration runs. Since real-time monitoring

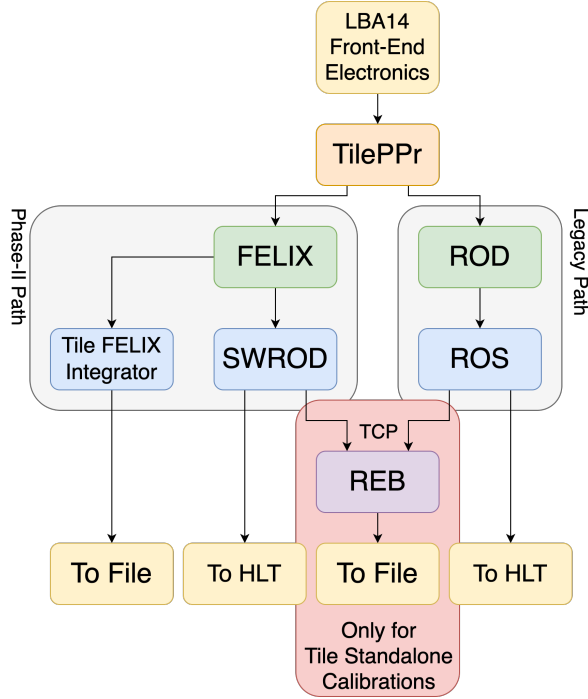


Figure 7.6: Data acquisition scheme for the demonstrator module in ATLAS.

is not yet available within the Tile Standalone partition, a dedicated set of scripts were developed to reconstruct and visualize the recorded data. Figure 7.7 presents the reconstructed signal from mini-drawer 0 of the Demonstrator module during one of the laser calibration runs.

To carry out the necessary developments and debugging, implementations in ATLAS must be scheduled during technical stops, which provide dedicated time windows without disrupting data-taking activities. Nevertheless, the tests performed within the ATLAS partition have been instrumental in validating the system’s readout path, successfully verifying the full data acquisition chain and demonstrating its readiness for the HL-LHC upgrade.

## MDO - HG Data (First 100 Events)

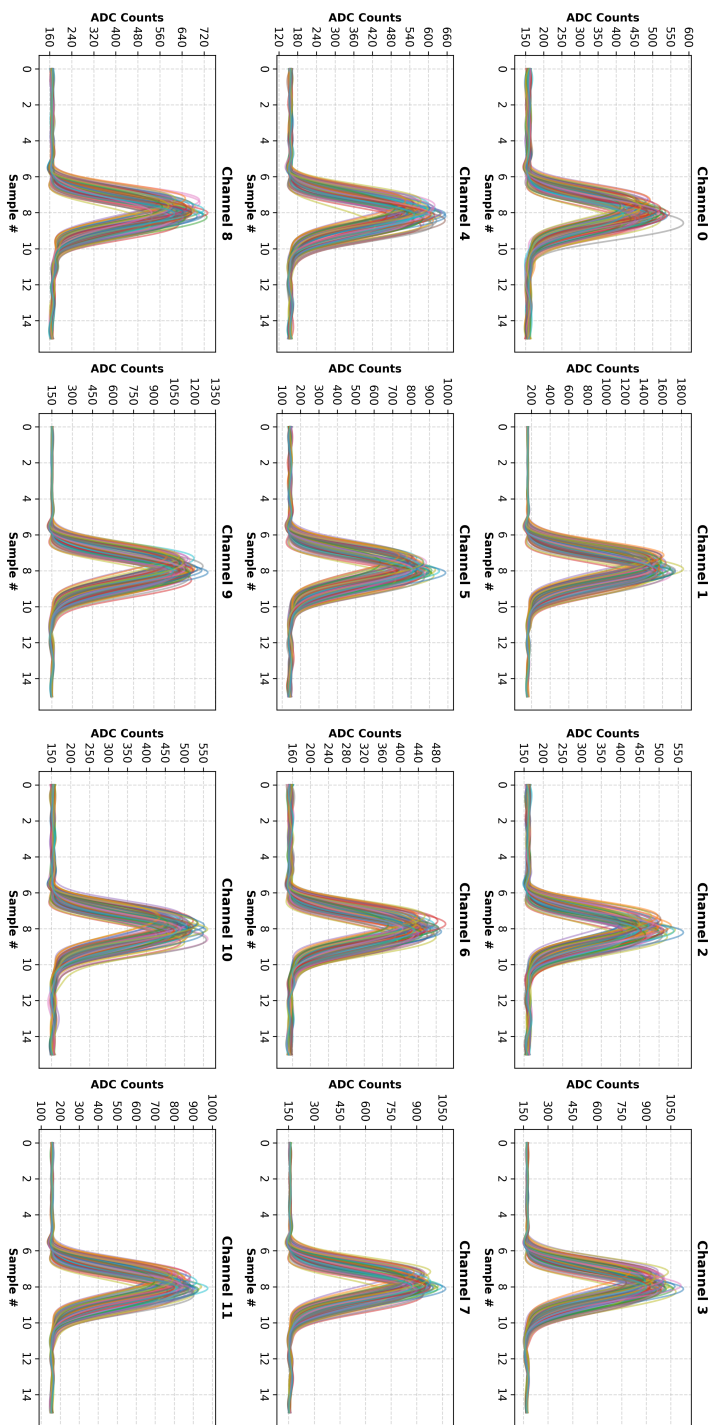


Figure 7.7: Reconstruction of laser calibration data showing high-gain signals from mini-drawers 0 from demonstrator module.

## Chapter 8

# Conclusions

This thesis has been developed within the framework of the ongoing upgrade of the ATLAS Tile Calorimeter for the HL-LHC era. The main objective was the design, implementation, and validation of new readout, control, and data acquisition systems capable of meeting the increased demands in data throughput, radiation tolerance, and timing precision introduced by HL-LHC conditions.

One of the main contributions of this work is the development and integration of a modernized TDAQ chain for TileCal. This includes the implementation of the FELIX and SWROD, which successfully replaced legacy hardware while offering a scalable, software-defined alternative compatible with high-bandwidth communication.

Further developments focused on custom SWROD plugins to enable seamless integration of data from both FELIX and legacy readouts. This approach ensures that testbeam campaigns data and data from the Tile Standalone partition within ATLAS can be merged into a single raw data file, simplifying subsequent processing and analysis.

A new integrator readout methodology was also introduced, based on FELIX and supported by a custom library that retrieve data from the CPMs

and save it to disk for offline analysis. Two software applications using this library were developed and validated during testbeam operations: one tailored for standalone usage—primarily for Cesium calibration—and another integrated within the TDAQ partition, operating in accordance with the FSM control flow.

In parallel, this thesis details the development of firmware, software and tools for the TileCoM, a compact System-on-Chip platform for the control and monitoring of off-detector and on-detector electronics. Through multiple iterations and debugging cycles, functional PetaLinux and AlmaLinux system images were developed, including the necessary FSBL modifications to support proper network initialization. A GitLab CI/CD pipeline was also established to automate the build process, enforce version control, and ensure reproducibility across development iterations. Integration of OPC UA and IPbus protocols enabled a flexible and robust remote control and monitoring infrastructure, further validating the TileCoMs readiness for deployment.

Additionally, to enable communication among all TilePPr modules housed within an ATCA shelf, a custom ATCA Switch Board was developed with an emphasis on reliable performance and system robustness. Validation tests, including bandwidth and error-rate measurements using tools like *iperf3*, confirmed the board’s ability to sustain 1 Gbps data transmission across all channels without errors.

All systems and developments presented in this thesis were rigorously validated through several successful testbeam campaigns. They were later integrated into the ATLAS Demonstrator module, where their functionality was confirmed under real detector operating conditions. This module was installed in the LBA14 position of the ATLAS detector in July 2019 and has been fully integrated since May 2020, operating continuously throughout Run 3 data-taking.

The successful testing and deployment of these developments in the Tile Standalone TDAQ partition, demonstrating the maturity and readiness for



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full-scale deployment during the HL-LHC era.

This thesis represents a significant contribution to the modernization of the TileCal electronics and DAQ systems. The designs, methodologies, and infrastructure introduced in this thesis will play a role in ensuring the long-term performance, reliability, and flexibility of the calorimeter’s readout and control systems, in line with the demanding requirements of the HL-LHC upgrade.

## Future work

Several areas of development remain open for future work, particularly as the HL-LHC commissioning phase approaches and the full detector integration is finalized.

The FELIX and SWROD systems will need to be scaled up and tested with multiple TileCal modules to ensure their proper functionality in large-scale configurations. These tests will be essential during the commissioning phase, as they will help verify the operational status of each module once inserted into the detector and ensure reliable data transmission from the cavern to the counting room (USA15).

Further developments in the TDAQ software system are required to accommodate the new electronics architecture. This includes the definition of updated partition schemas, along with the development of new applications for the control, configuration, and monitoring of TilePPr modules. While some work in this direction has already begun, particularly concerning the TilePPr design, these developments were not presented in this thesis due to their early stage.

*TileFELIXIntegrator* libraries may also require adaptation to remain compatible with upcoming changes in the TDAQ framework, ensuring their continued use for calibration and monitoring tasks.

The TileCoM module is still undergoing hardware development. A new revision is expected to address current integration issues with the ACBB board.

Once this hardware is available, further software development will be required, particularly to enhance the OPC UA server, integrating all off-detector monitoring data. In parallel, an on-detector OPC UA server should be developed to monitor front-end electronics directly. The operating system image and file system will also need to be maintained and potentially adapted to future changes, such as the adoption of AlmaLinux or other distributions at the start of Run 4. The existing automation infrastructure should be preserved to guarantee reproducibility and ease of deployment.

Regarding the custom ATCA Switch Board, a potential upgrade path involves the development of a new Gigabit Ethernet mezzanine module capable of supporting higher data rates. The current design includes provisions to utilize the ATCA fabric interface, which can be exploited to meet these future requirements.

Finally, comprehensive testing and validation of the FELIX and SWROD integration within the ATLAS partition should be carried out. This work is still in progress at the time of writing this thesis.

Gaining operational experience and identifying potential failure modes during this phase will be essential to ensuring a smooth start of Run 4 and guaranteeing system stability for the HL-LHC operation.

## Chapter 9

# Resum

Aquesta tesi s'emmarca dins del projecte d'actualització del *Tile Calorimeter* (TileCal) del detector *A Toroidal LHC ApparatuS* (ATLAS), en preparació per a la fase d'alta lluminositat del Gran Col·lisionador d'Hadrons (*High-Luminosity LHC* (HL-LHC)). L'objectiu principal del projecte és el desenvolupament de *hardware*, *software* i *firmware* per al *Data AcQuisition* (DAQ) i *Detector Control System* (DCS) del TileCal, abastant tant la recepció i tractament de dades com el control de l'electrònica associada a aquesta adquisició.

Aquesta tesi descriu el disseny, implementació i validació del sistema d'adquisició de dades del TileCal mitjançant l'ús dels sistemes *Front-End Link eXchange* (FELIX) i *SoftWare ReadOut Driver* (SWROD). A més, es presenten altres desenvolupaments realitzats en el marc d'aquesta tesi relacionats amb l'actualització del TileCal, com la depuració, implementació i validació del *firmware* i *software* del *Tile Computer-on-Module* (TileCoM) —un petit ordinador encastat que s'allotjarà en l'electrònica de lectura i que s'encarrega del control i la monitorització dels components de *front-end* i *back-end*.

També s'inclou el disseny i validació d'un *switch* compatible amb l'estàndard *Advanced Telecommunications Computing Architecture* (ATCA), destinat a permetre una interconnexió eficient entre les diferents targetes de

lectura de dades del detector.

El sistema dissenyat s'ha provat i integrat en el Demonstrator, un mòdul prototip que incorpora els desenvolupaments electrònics més recents i que actualment funciona dins de l'experiment ATLAS. Per tal de validar-ne el funcionament i estudiar-ne el rendiment, s'han realitzat nombroses proves en bancs de treball (*test benches*) i campanyes de presa de dades amb feixos de partícules (*testbeams*).

## 9.1 Introducció

El *European Organization for Nuclear Research* (*Conseil Européen pour la Recherche Nucléaire*) (CERN) és el centre de referència per a la investigació fonamental en física de partícules. Fundat en 1954, el CERN es troba situat en la frontera franco-suïssa, prop de Ginebra, Suïssa.

La missió principal del CERN és estudiar els constituents fonamentals de la matèria i les forces que regixen les seues interaccions. Per a dur-ho a terme, el CERN gestiona una àmplia xarxa d'acceleradors i detectors de partícules, facilitant així experiments innovadors i descobriments pioners en el camp de la física de partícules.

En el centre dels esforços del CERN es troba el *Large Hadron Collider* (LHC), l'accelerador de partícules més potent del món, conegut per la seua capacitat d'accelerar feixos de protons a energies sense precedents i fer-los col·lidir a velocitats pròximes a la de la llum. Estén el seu túnel circular al llarg de 27 quilòmetres de circumferència i s'endinsa fins a 100 metres baix terra, travessant la frontera entre França i Suïssa.

En el seu nucli, l'LHC utilitza potents imants superconductors dissenyats amb precisió per a guiar feixos de protons cap a col·lisions frontals, aconseguint una energia en el centre de masses de  $\sqrt{s} = 13.6$  TeV.

Aquesta energia de col·lisió es complementa amb una lluminositat instantània de  $\mathcal{L} = 1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ , creant unes condicions experimentals sense precedents.

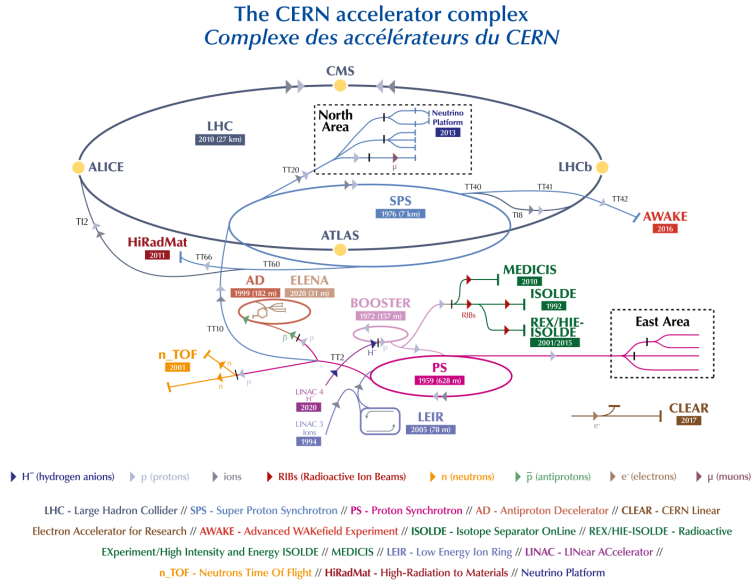


Figure 9.1: Complex d'acceleradors al CERN.

El camí cap a aquestes energies de col·lisió comença molt abans dins del complex d'acceleradors del CERN, com es pot veure a la Figura 9.1, una extensa xarxa d'acceleradors interconnectats. El procés s'inicia amb el *Linear Accelerator 4* (Linac4) i el *Proton Synchrotron Booster* (PSB), que actuen com les primeres etapes impulsant el feix de protons fins a una energia de 1.4 GeV. A continuació, el *Proton Synchrotron* (PS) pren el control, elevat l'energia del feix fins als 25 GeV. Posteriorment, el *Super Proton Synchrotron* (SPS) accelera encara més els protons fins a 450 GeV abans d'injectar-los finalment en l'LHC.

### 9.1.1 Experiment ATLAS

El ATLAS és un dels dos detectors de propòsit general del LHC dissenyat per a estudiar els productes de les col·lisions p-p en el LHC, abastant un ampli espectre d'estudis en física, des del bosó de Higgs fins a l'exploració de

dimensions extra i possibles components de la matèria fosca. Tot i compartir objectius científics similars amb l'experiment *Compact Muon Solenoid* (CMS), ATLAS utilitza solucions tècniques diferents i un disseny de sistema d'imants únic. Amb un pes de 7000 tones i unes dimensions de 46 metres de longitud i 25 metres tant d'altura com d'amplada, el detector ATLAS (Figura 9.2) és el detector de partícules de major volum mai construït.

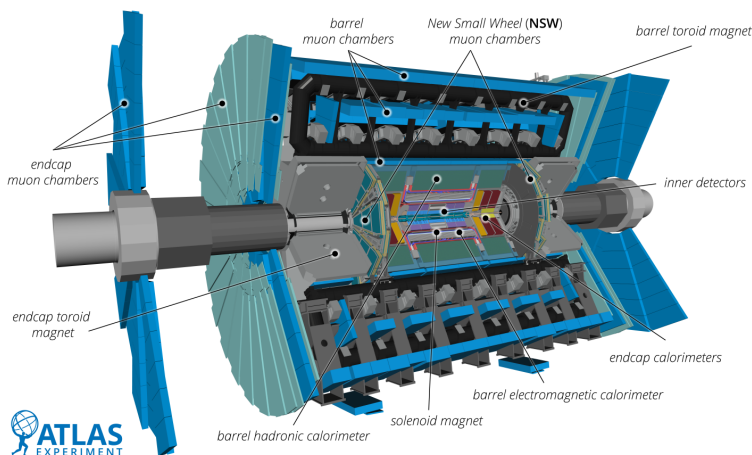


Figure 9.2: L'experiment ATLAS.

En el centre de ATLAS, les partícules del LHC col·lideixen, generant restes de col·lisió en forma de noves partícules que es dispersen en totes direccions des del punt de col·lisió. Sis subsistemes de detecció diferents, disposats en capes al voltant del punt de col·lisió, enregistren meticulosament les trajectòries, el moment i l'energia d'aquestes partícules, facilitant-ne la identificació individual. Un sistema d'imants dins d'ATLAS corba les trajectòries de les partícules carregades, permetent una mesura precisa del seu moment.

Les interaccions dins del detector ATLAS produeixen un enorme volum de dades. Per a gestionar aquesta quantitat d'informació, ATLAS fa ús d'un sofisticat sistema de *trigger* per a discernir quins esdeveniments han de ser registrats i quins han de ser descartats. Posteriorment, els sistemes d'adquisició de dades i computació analitzen els esdeveniments de col·lisió enregistrats.

L'*Inner Detector* (ID) d'ATLAS està situat al voltant del tub de feix, i ha sigut dissenyat específicament per a la traçabilitat i identificació de vèrtexs, rastrejant les trajectòries de les partícules carregades produïdes en les col·lisions. Al voltant de l'ID es troba un imant solenoidal, el qual corba les trajectòries de les partícules carregades. Aquesta curvatura es fa servir per a calcular el moment de les partícules.

Envoltant l'ID, el calorímetre de *Liquid Argon* (LAr), que actua com a calorímetre electromagnètic, i el TileCal, que funciona com a calorímetre hadrònic, treballen conjuntament per a mesurar l'energia dipositada per les partícules i reconstruir-ne les direccions. La capa més externa d'ATLAS inclou el *Muon Spectrometer* (MS) i un imant toroidal, on un sistema de rastreig de muons segueix la trajectòria dels muons més enllà dels calorímetres. Tres imants toroidals superconductors d'aire envolten el detector ATLAS, el qual corben les trajectòries de les partícules carregades.

Durant el *Long Shutdown 2* (LS2), realitzat entre 2019 i 2021, es va dur a terme el projecte de millora de Fase-I. Les actualitzacions de Fase-I es van implementar per a satisfer les demandes creixents del *Run 3* de la captura de dades del LHC. Aquesta fase de millora, completada abans de l'inici del *Run 3*, va incloure millores en el detector i en els sistemes de *trigger*.

Les millores clau en la Fase-I es van centrar en l'actualització del sistema de *trigger* de nivell 1 (*Level-1 (First-level trigger)* (L1)), incloent la substitució de la *Small Wheel* en l'espectròmetre de muons pel *New Small Wheel* (NSW). El NSW es va dissenyar per a proporcionar un millor rastreig i reduir els falsos *triggers* de muons. El calorímetre de LAr també va rebre millores significatives amb la introducció d'un sistema de *trigger* digital, augmentant la granularitat i la resolució energètica, millorant així l'eficiència del *trigger* d'electrons i fotons.

Pel que fa a la distribució *Trigger, Timing, and Control* (TTC), es va introduir el mòdul *ATLAS Local Trigger Interface* (ALTI). L'ALTI és un únic mòdul VMEbus dissenyat per a substituir diversos mòduls antics. La funció principal de l'ALTI és proporcionar una interfície entre el *Central Trigger*

*Processor* (CTP) de nivell 1 i el sistema local TTC dels subdetectors.

Aquestes millores tenien com a objectiu gestionar taxes d'esdeveniments més altes mentre es mantenia el rendiment i la precisió del detector. Els nous sistemes es van posar en funcionament durant el 2022, amb la integració completa en el detector ATLAS en 2023.

### **Sistema de Trigger i Adquisició de Dades**

El sistema *Trigger and Data Acquisition* (TDAQ) ha evolucionat significativament des del *Run 1* i *Run 2* per a satisfer les demandes creixents de lluminositat i taxa de dades en el LHC. Inicialment dissenyat per a manejar taxes d'esdeveniments més baixes i criteris de selecció més simples, ha sigut contínuament actualitzat amb nous components de *hardware*, *software* i algorismes per a millorar l'eficiència de selecció d'esdeveniments, la precisió i la gestió de dades. Durant el *Run 3* (2022-2026), el sistema TDAQ va incorporar noves tecnologies i configuracions (Figura 9.3), aprofitant la millora en la resolució del detector i en els temps de resposta per a analitzar processos físics més complexos, tot mantenint un rendiment òptim sota taxes de col·lisió més altes.

El L1 es basa en dos sistemes independents amb electrònica personalitzada: el *Level-1 Calorimeter* (L1Calo) i el *Level-1 Muon* (L1Muon). El sistema *Level-1 Topological Processor* (L1Topo) aplica seleccions topològiques utilitzant informació cinemàtica dels objectes reconstruïts en L1Calo i L1Muon. La decisió del L1 es pren en el CTP, que integra entrades de diversos sistemes, incloent *Minimum Bias Trigger Scintillators* (MBTS), *ATLAS Forward Proton* (AFP), *Absolute Luminosity For ATLAS* (ALFA), *Luminosity Cherenkov Integrating Detector 2* (LUCID-2) i *Zero Degree Calorimeter* (ZDC). El CTP també gestiona el *deadtime* per a controlar el nombre d'acceptacions successives del L1.

Els esdeveniments acceptats, amb una taxa màxima de lectura del detector de 100 kHz i una latència fixa inferior a 2.5 microsegons, passen al *High-Level Trigger* (HLT), un sistema basat en *software* que reconstrueix esdeveniments



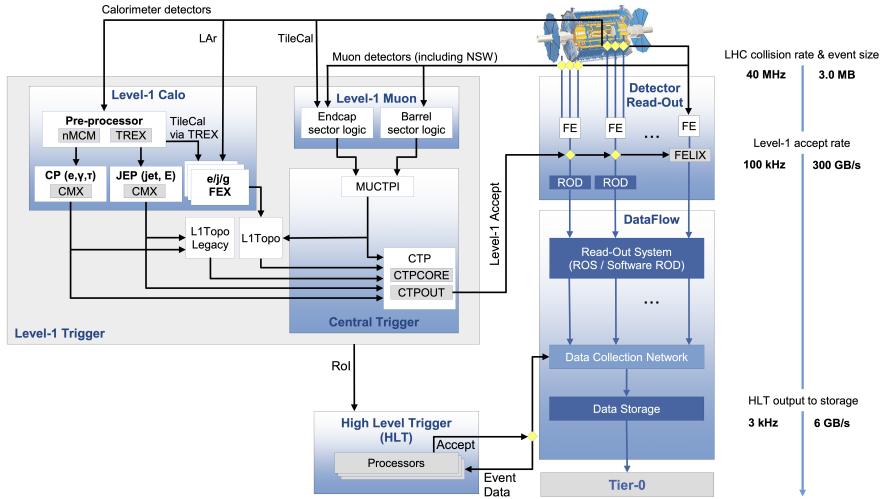


Figure 9.3: El sistema TDAQ d'ATLAS en Run 3.

amb major detall, ja siga en tot el detector o en *Regions-of-Interest* (RoIs) seleccionades pel L1. Per al *Run 3*, el HLT es va redissenyar per a permetre execució *multi-threaded*. El L1 redueix la taxa d'esdeveniments de 40 MHz a 100 kHz, mentre que l'HLT aplica filtres addicionals fins a reduir-la a uns 3 kHz.

El sistema DAQ gestiona els fragments d'esdeveniments generats pels detectors, els emmagatzema temporalment fins que es prenga una decisió de *trigger* i, posteriorment, construeix esdeveniments complets per a emmagatzemar-los permanentment. A més, proporciona les eines de control, configuració i monitorització necessàries per al funcionament del detector.

### 9.1.2 Calorímetre Hadrònic TileCal

El detector TileCal dins d'ATLAS és un calorímetre de mostreig que utilitza acer com a material absorbent i rajoles de centelleig com a medi actiu. Situat darrere del calorímetre electromagnètic LAr, cobreix la regió de  $|\eta| < 1.7$ .

TileCal consta d'un barril longitudinal central, de 5.6 metres de longitud,

i dos barrils extesos, cadascun de 2.6 metres de llarg. Cada barril està dividit azimutalment en 64 sectors de mida  $\Delta\phi \sim 0.1$ , formats per plaques d'acer i rajoles de centelleig.

La disposició de les rajoles de centelleig, orientades tant radialment com normalment a l'eix del feix, en combinació amb la lectura de les vores de les rajoles mitjançant fibres de *WaveLength Shifting* (WLS), garanteix una cobertura calorimètrica azimutal gairebé contínua. Aquestes fibres WLS es reuneixen en feixos que defineixen 5182 cèl·lules calorimètriques, les quals són llegides per 9852 *PhotoMultiplier Tube* (PMT).

L'electrònica de *front-end* es troba dins dels *super-drawers*, que contenen els PMT, el sistema de digitalització i l'electrònica d'adquisició de dades. Els PMTs transformen la llum en càrrega elèctrica i la senyal es processa mitjançant targetes 3-in-1, que amplifiquen i conformen la senyal abans de la digitalització.

L'electrònica de fora del detector, situada a *Underground Service Area 15 (ATLAS Counting Room)* (USA15), inclou els sistemes *Read Out Driver* (ROD) i TTC. Els mòduls ROD reben dades des de vuit *super-drawers* mitjançant enllaços òptics i les processen abans d'enviar-les al sistema DAQ d'ATLAS. El sistema TTC gestiona la sincronització i el control del detector.

El flux de dades comença amb la detecció de la llum emesa per les rajoles de centelleig i la conversió en senyals digitals, que són transmeses al sistema de *trigger*. Quan es genera un senyal de *Level-1 Accept signal* (L1A), les dades seleccionades són enviades a la interfície del *off-detector*, on es processen i emmagatzemen. La taxa de lectura està limitada per un senyal de control de sobrecàrrega (*busy signal*) que evita la saturació del sistema.

Per a la calibració, el calorímetre està equipat amb un sistema làser, un *Charge Injection System* (CIS), i una font radioactiva de  $^{137}\text{Cs}$ , assegurant una calibració precisa de la resposta del detector a l'escala electromagnètica. L'estructura dels mòduls de TileCal s'il·lustra en la Figura 9.4.

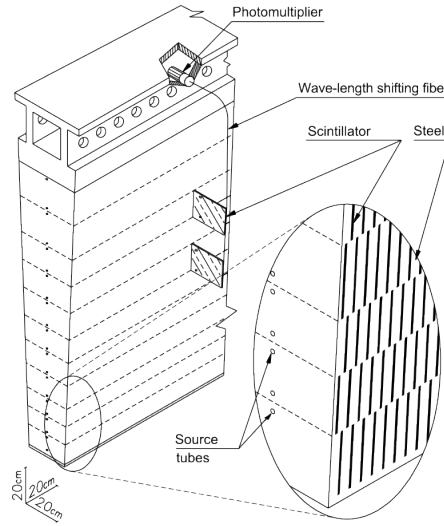


Figure 9.4: Esquema que mostra com s'integren l'assemblatge mecànic i la lectura òptica del Calorímetre de Tile. Es representen els diferents components de la lectura òptica, incloent les rajoles, les fibres i els fotomultiplicadors.

### 9.1.3 Millores al *High Luminosity LHC* i a l'experiment ATLAS

EL HL-LHC representa una actualització important del LHC, destinada a millorar-ne la capacitat per explorar els aspectes fonamentals de la física de partícules. Prevista per a completar-se durant el *Long Shutdown 3* (LS3) (2026-2030) (Figura 9.5), aquesta millora augmentarà la lluminositat instantània fins a unes 7.5 vegades superior al disseny original de l'LHC. Això generarà una mitjana de 200 col·lisions inelàstiques per creuament de feix (en comparació a les 60-70 actuals), permetent obtenir un volum de dades molt elevat per a estudis detallats del Model Estàndard i possibles fenòmens més enllà d'aquest.

En paral·lel, el detector ATLAS està rebent una actualització integral, coneguda com la Fase-II, per adaptar-se a les noves condicions operacionals. Aquestes millores són essencials per gestionar l'augment de lluminositat i la pujada del nombre d'esdeveniments per creuament de feix. Per a fer front a



Figure 9.5: Planificació del LHC / HL-LHC. Actualitzat Gener 2025.

aquests reptes, ATLAS millorarà la granularitat del detector, implementarà una nova arquitectura TDAQ capaç de gestionar taxes de *trigger* més elevades i instal·larà una electrònica de *front-end* més resistent a la radiació.

Diversos subdetectors, com l'*Inner Detector*, el calorímetre LAr *Forward* i les *Forward Muon Wheels*, requeriran una substitució completa a causa del dany per radiació. Altres components, com els calorímetres i les cambres de muons, només necessitaran millores electròniques per suportar l'augment de flux de dades i les noves condicions de radiació.

### Actualització del TDAQ

El sistema TDAQ de la Fase-II ha estat dissenyat per gestionar les exigències complexes de l'HL-LHC. L'arquitectura es divideix en tres subsistemes principals: el sistema de *Trigger* de Nivell-0 (*Level-0 (Trigger System) (L0)*), el sistema d'Adquisició de Dades (DAQ) i el sistema de filtrat d'events (*Event Filter (EF)*).

Les dades del detector ATLAS s'integren en el sistema a través de tres categories principals: el *Inner Tracker (ITk)* (incloent detectors de píxels i

tires), els Calorímetres (LAr i TileCal) i el Sistema de Muons (*Monitoring Drift Tube* (MDT), *Resistive Plate Chamber* (RPC), *Thin Gap Chamber* (TGC) i NSW). Aquestes dades són processades per l'electrònica específica de cada detector, que s'encarrega tant de la lectura com de la preparació inicial de les dades de *trigger*.

El sistema de *trigger* de Nivell-0 (L0) inclou components com *Level-0 Calorimeter* (L0Calo), *Level-0 Muon* (L0Muon), el *Trigger* Global i el *Trigger* Central. L0Calo utilitza dades dels calorímetres per identificar electrons, leptons tau, jets i calcular l'energia transversal perduda  $E_T^{miss}$ , mentre que L0Muon processa informació de totes les subsistemes de muons i de les cèl·lules externes de TileCal. El sistema de *Trigger* Global aplica algorismes avançats per refinar la selecció d'esdeveniments, integrant dades de gran granularitat i calculant quantitats físiques complexes en una finestra de 10  $\mu s$ . El CTP redueix la taxa d'esdeveniments de 40 MHz a 1 MHz abans d'enviar les dades a les següents etapes d'adquisició.

Després de la decisió del L0, les dades passen al sistema DAQ, on es processen amb components com FELIX, que actua com a interfície entre els enllaços de lectura personalitzats del detector i la xarxa DAQ, i els *Data Handlers*, que s'encarreguen del formatat i monitorització de les dades.

L'última etapa del procés és el sistema EF, que consta d'una granja de processament i un sistema *Hardware Tracking for the Trigger* (HTT) dedicat a l'anàlisi d'alta velocitat. Aquest sistema redueix la taxa d'esdeveniments fins a 10 kHz, seleccionant només els esdeveniments més rellevants per a l'emmagatzematge permanent.

### **Actualització del Calorímetre Hadrònic TileCal**

La Fase-II comportarà una renovació completa de l'electrònica de lectura del TileCal per resistir l'augment de radiació i integrar-se amb la nova arquitectura del TDAQ. L'electrònica del *off-detector* serà responsable de la lectura del detector i la transmissió de dades pre-processades als sistemes de *trigger*

a la freqüència operativa de l'LHC, mentre que les mostres de dades seran emmagatzemades fins a rebre un senyal *Level-0 Accept signal* (LOA) (Figura 9.6).

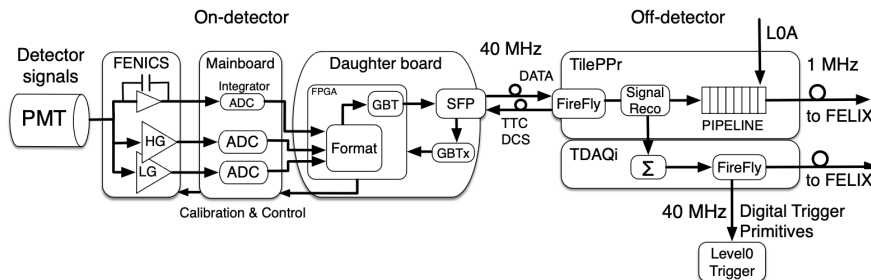


Figure 9.6: Esquema del camí del senyal i les dades en l'actualització per a la Fase-II del TileCal.

Per suportar la nova arquitectura, el nombre d'enllaços òptics entre el *front-end* i el *back-end* augmentarà de 256 a 4096, amb una amplada de banda per enllaç que passarà de 800 Mbps a 160 Gbps, tal com es mostra en la Taula 9.1.

L'electrònica del TileCal s'instal·larà en 256 *super-drawers* (128 al barril llarg i 128 al barril estès) de tres metres de llarg, muntats en els mòduls del calorímetre. Cada *super-drawer* està dividit en quatre (per al barril llarg) o tres (per al barril estès) *mini-drawers* independents, que allotgen els components electrònics i proporcionen serveis elèctrics, òptics i de refrigeració.

| Baixades              | Actual        | Fase-II   |
|-----------------------|---------------|-----------|
| # enllaços            | 256           | 2048      |
| Ample de banda/enllaç | 80 Mbps (TTC) | 4.8 Gbps  |
| Pujades               | Actual        | Fase-II   |
| # enllaços            | 256           | 4096      |
| # plaques             | 32 (VME)      | 32 (ATCA) |
| # bastidors           | 4 (VME)       | 4 (ATCA)  |
| Ample de banda/enllaç | 800 Mbps      | 160 Gbps  |
| Ample de banda/placa  | 6.4 Gbps      | 1.28 Tbps |
| Ample de banda total  | 165 Gbps      | 40 Tbps   |

Table 9.1: Comparació entre els sistemes de lectura actual i de la Fase-II.

Els *mini-drawers* contenen l'electrònica necessària per al processament del senyal, incloent PMTs, *Front-End board for the New Infrastructure with Calibration and Signal Shaping* (FENICS), *MainBoard* i *DaughterBoard*. La *MainBoard* canalitza les dades cap a la *DaughterBoard*, que gestiona la comunicació amb el *back-end*. L'electrònica s'ha dissenyat per resistir la radiació i garantir un funcionament fiable durant tota la vida útil del detector.

El sistema *off-detector* del TileCal estarà compost per 32 mòduls *Tile Pre-Processor* (TilePPr) (compostos a la vegada per la *ATCA Carrier BaseBoard* (ACBB) i els *Compact Processing Module* (CPM)) i 32 mòduls *Trigger and Data Acquisition interface* (TDAQi). El TilePPr actua com a interfície entre l'electrònica en el detector i els sistemes centrals de l'experiment ATLAS, gestionant les altes taxes de dades requerides per a l'HL-LHC (Figura 9.7).

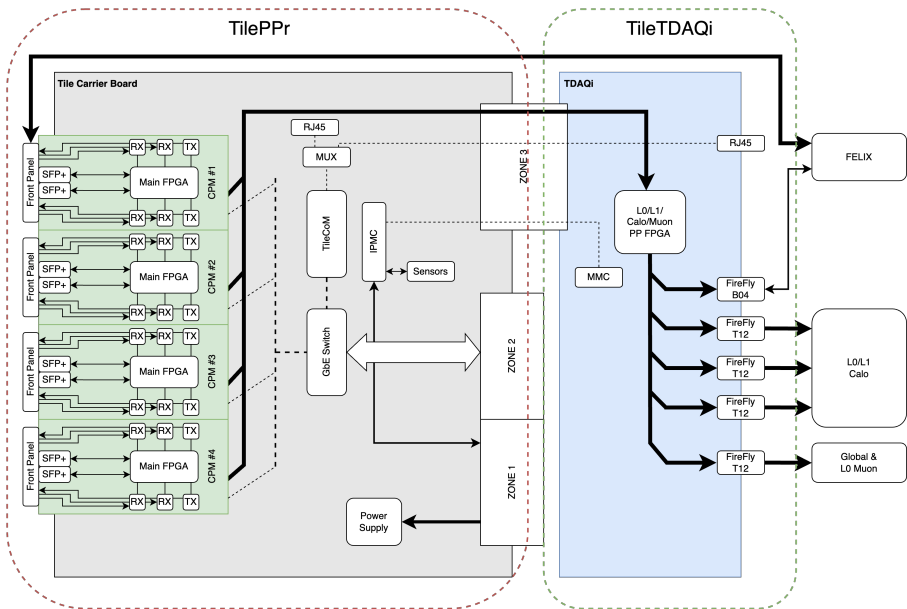


Figure 9.7: Diagrama del sistema off-detector del TileCal.

## 9.2 Desenvolupaments al sistema d'adquisició de dades

Diferents desenvolupaments tenen lloc en el sistema d'adquisició de dades TDAQ de l'experiment ATLAS, en el marc de l'actualització per a la Fase-II de l'HL-LHC. Aquestes millores són essencials per adaptar-se a les noves condicions d'operació, que impliquen una taxa de col·lisions molt superior, així com requeriments més estrictes pel que fa a latència, ample de banda i tolerància a la radiació.

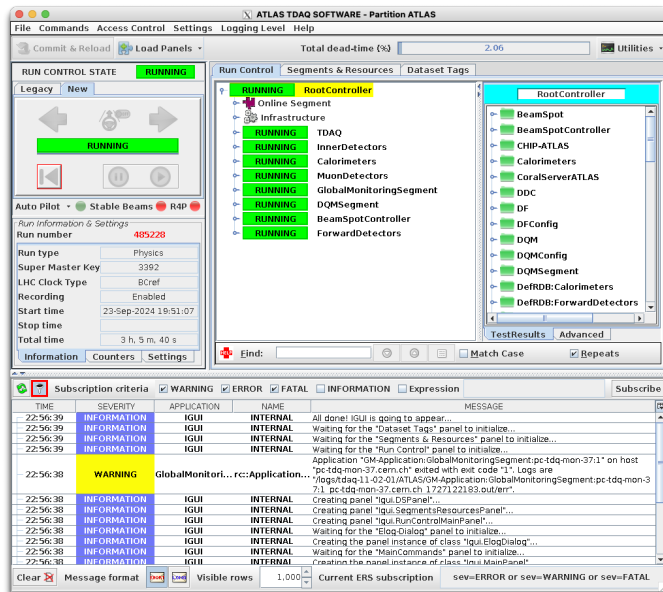


Figure 9.8: El panell del *software* TDAQ d'ATLAS.

El *software* del TDAQ (Figura 9.8) configura una infraestructura distribuïda i jeràrquica que opera sobre milers de nodes Linux i executa desenes de milers d'aplicacions. Aquest sistema està dissenyat per garantir un control robust, una configuració flexible i una monitorització eficaç de tot el procés de presa de dades. Es basa en tres subsistemes principals —configuració, control i monitoratge— amb una arquitectura centrada en serveis que treballen de



manera coordinada per assegurar una execució eficient i segura de les aplicacions distribuïdes.

La base de dades *Object Kernel Support* (OKS) defineix la jerarquia i el comportament dels elements implicats en una presa de dades: particions, segments, aplicacions, recursos i conjunts de recursos. Cada partició pot operar de manera independent i està formada per segments auto-contenits, cadascun amb les seues pròpies aplicacions i recursos. Aquesta arquitectura modular proporciona una gran flexibilitat, facilita la reutilització, l'aïllament d'errors i la configuració de múltiples escenaris d'operació.

El sistema de control, implementat mitjançant el *Run Control*, segueix una màquina d'estats finits *Finite State Machine* (FSM) distribuïda que sincronitza les transicions d'estat de totes les aplicacions i segments. A més, el sistema incorpora mecanismes avançats de recuperació d'errors, com la reintegració sense aturar (*stopless recovery*) i la desconnexió automàtica de components defectuosos (*stopless removal*).

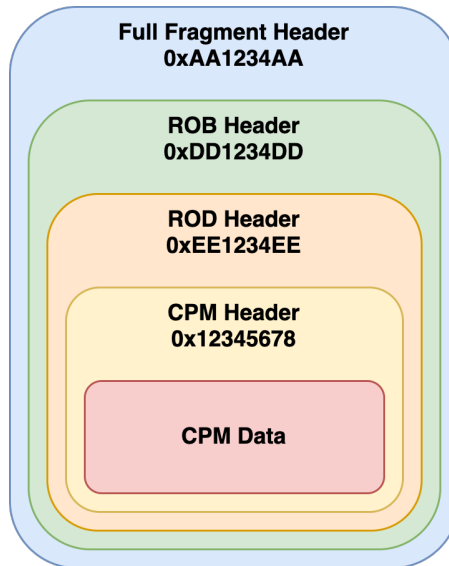


Figure 9.9: Esquema actualitzat del format del paquet de dades d'ATLAS per a l'actualització de Fase-II del Tile Calorimeter.

El sistema d'adquisició de dades utilitza un format jeràrquic de paquets (Figura 9.9), que abasta des dels fragments bàsics ROD fins a la construcció dels fragments complets d'esdeveniment. Cada nivell de fragment conté informació específica sobre la configuració, la identificació de l'esdeveniment i les dades adquirides. Amb la Fase-II, entra en funcionament un nou format que incorpora més mostres per canal i afegeix metadades addicionals. Aquest disseny millora l'eficiència en la reconstrucció i permet comparar de manera directa les dades entre els sistemes llegat i els nous sistemes basats en FELIX.

Una de les innovacions més destacades és la introducció de FELIX, una interfície comuna al detector ATLAS que substitueix la lectura basada en *hardware* dedicat. FELIX utilitza targetes *Peripheral Component Interconnect Express* (PCIe) d'alt rendiment instal·lades en servidors comercials, habilitant una comunicació bidireccional entre l'electrònica de *front-end* i el sistema d'adquisició mitjançant enllaços òptics.

El SWROD reemplaça funcionalment els antics mòduls ROD i *ReadOut System* (ROS), agregant fragments de dades, assegurant la seua integritat i gestionant la comunicació amb el sistema HLT. Es desenvolupa un plugin específic per a TileCal que permet empaquetar les dades en un format compatible amb el sistema llegat, afavorint així la comparació entre les dues arquitectures durant les campanyes de validació i calibracions. També es desenvolupa un complement personalitzat dins del SWROD per enviar dades a través de *Transmission Control Protocol* (TCP) al mòdul *ROS Event Builder* (REB), responsable d'agregar les dades dels diferents mòduls del detector en un únic arxiu durant les campanyes de *testbeam* i durant les fases de calibració de TileCal dins d'ATLAS (Figura 9.10).

El sistema de lectura de l'integrador s'utilitza tant per a la monitorització de la lluminositat com per a les calibracions amb fonts radioactives. Inicialment gestionat amb *Internet Protocol bus* (IPbus), aquest sistema migra a una arquitectura basada en FELIX, que permet una lectura contínua i paral·lela al sistema de triggers. Per donar suport a aquesta funcionalitat, es desenvolupa

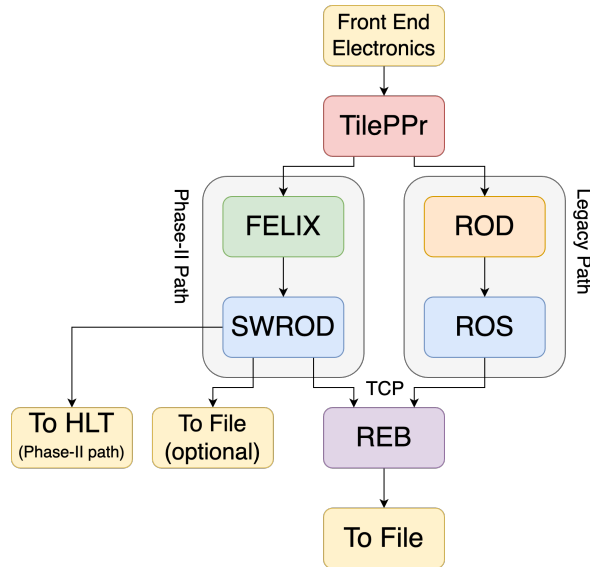


Figure 9.10: Diagrama que il·lustra el camí de lectura de dades per a l'actualització de Fase-II, funcionant en paral·lel amb el camí de dades actual, utilitzat per a les calibracions independents del Tile i les campanyes de *testbeam*.

una llibreria en C++ (*TileFelixIntegrator*) amb implementacions tant integrades al sistema TDAQ com en mode autònom. Aquesta llibreria s'encarrega de gestionar les connexions, rebre i emmagatzemar les dades i garantir un processament eficient mitjançant una arquitectura *multithread* i basada en *callbacks*.

Per al postprocessament, es desenvolupa un *software* específic de reconstrucció que llig els fitxers binaris generats pel sistema de lectura de l'integrador, sincronitza els paquets, extreu la informació rellevant i l'escriu en arxius *ROOT* estructurats amb *TTree*. Aquest procés assegura la integritat de les dades i permet una anàlisi detallada de la resposta del detector tant en condicions de funcionament regular com durant campanyes de proves o calibració.

### 9.3 Desenvolupaments al sistema de control del detector

En el marc de l'actualització de l'electrònica del detector de TileCal, es desenvolupa el mòdul TileCoM, un sistema compacte basat en *System-on-Chip* (SoC), dissenyat per a realitzar tasques de control i monitoratge sobre l'electrònica fora del detector. Proporciona accés remot al sistema TilePPr, permetent la programació de les *Field-Programmable Gate Array* (FPGA), la distribució local de rellotge i la supervisió de l'estat del sistema. A més, facilita la lectura contínua dels sensors de DCS a través de la infraestructura de TileCal, garantint un funcionament robust i la capacitat de resposta en temps real.

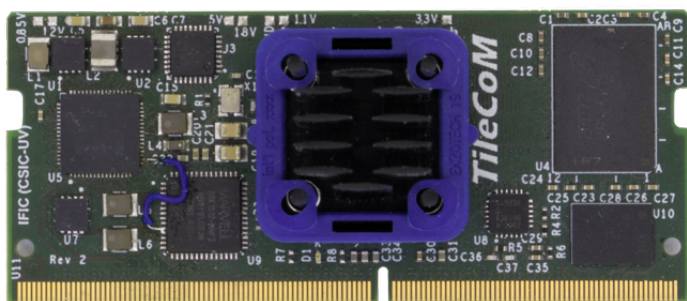


Figure 9.11: Imatge de la placa TileCoM versió 1.2.

El *hardware* del TileCoM (Figura 9.11), desenvolupat a l'*Institut de Física Corpuscular* (IFIC), utilitza un SoC *Advanced Micro Devices* (AMD) Zynq UltraScale+ ZU2CG, que integra un processador *Advanced RISC (Reduced Instruction Set Computer) Machines* (ARM) Cortex-A53 i lògica programable. La placa, de  $3 \times 7$  cm i 10 capes de *Flame Retardant 4* (FR4), incorpora 2 GB de *Double Data Rate 4* (DDR4) *Random-Access Memory* (RAM), memòria *Quad Serial Peripheral Interface* (QSPI), ranura microSD, dues interfícies *Gigabit Ethernet* (GbE), i diverses connexions com *Universal Serial*

*Bus* (USB), *Serial Peripheral Interface* (SPI), *Inter-Integrated circuit* (I2C) i *Universal Asynchronous Receiver/Transmitter* (UART).

El disseny de *firmware* es desenvolupa amb Vivado, integrant el bloc *Processing System* (PS) del SoC i implementant interfícies com I2C mitjançant la interconnexió *Advanced eXtensible Interface* (AXI), per tal de comunicar-se amb l'*Intelligent Platform Management Controller* (IPMC) de l'ACBB i obtenir informació de la posició de la targeta dins del bastidor ATCA. El disseny és modular i permet afegir funcionalitats a mesura que es completa el depurat del sistema.

Pel que fa al *software*, el TileCoM requereix un sistema operatiu Linux per tal d'integrar-se amb el sistema DCS. El procés d'arrencada segueix una seqüència multietat on s'inicialitza el *hardware* mitjançant el *First Stage Boot Loader* (FSBL), que configura els recursos essencials i, en aquest cas, programa via I2C el generador de rellotge per a generar el rellotge de 125 MHz necessari per a la connexió Ethernet. Aquest pas és fonamental per assegurar la funcionalitat de xarxa abans de carregar el nucli del sistema.

La imatge del sistema s'elabora amb PetaLinux, basat en el projecte Yocto, que permet configurar i generar una distribució personalitzada per al *Multiprocessor System on Chip* (MPSoC). La integració amb Vivado permet importar el disseny de *hardware* i generar els controladors corresponents.

A causa de la migració institucional cap a AlmaLinux, impulsada per CERN, s'adapta un sistema dual on es genera un sistema d'arxius (*rootfs*) per a AlmaLinux utilitzant un script desenvolupat per l'equip de SoC del CERN i amb modificacions per a fer una imatge preparada per a ser utilitzada amb totes les ferramentes necessàries, mentre que el nucli del sistema (*kernel*) continua sent el generat per PetaLinux. Aquesta combinació permet conservar compatibilitat amb les exigències del sistema TDAQ i complir amb les polítiques de seguretat i manteniment.

El desenvolupament es gestiona mitjançant Git i GitLab, amb dos repositoris diferenciats per al disseny de *hardware* (Vivado) i per a la imatge de

sistema Linux. Es configura un flux complet de *Continuous Integration / Continuous Deployment* (CI/CD) amb GitLab (Figura 9.12), on cada canvi al disseny de *hardware* genera automàticament els fitxers necessaris i activa la construcció de la imatge del sistema en el repositori de *software*. Aquest procés s'executa mitjançant *Docker* i GitLab Runners, assegurant reproduïbilitat i aïllament durant la construcció.

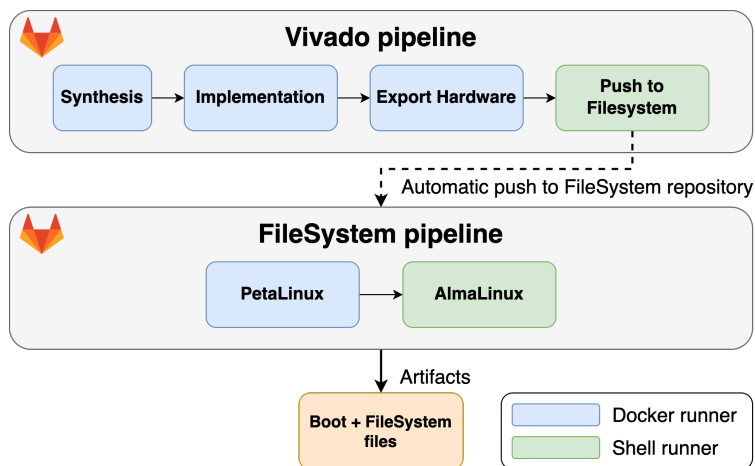


Figure 9.12: Diagrama que il·lustra el flux complet de treball CI/CD implementat per als repositoris del TileCoM.

Per a la supervisió i control, el TileCoM integra una arquitectura basada en IPbus i *Open Platform Communications Unified Architecture* (OPC UA). Mitjançant IPbus, accedeix als CPMs per recuperar dades de sensors interns i altra informació rellevant. Aquesta informació es publica mitjançant un servidor OPC UA, generat amb el marc Quasar, que permet modelar la jerarquia de dispositius i publicar-la de manera estàndard. S'implementen dos servidors diferenciats: un per al monitoratge del sistema TilePPr i un altre per al sistema *on-detector*, amb accés a les dades emmagatzemades en memòria dins dels CPMs.

Per tant de poder provar la funcionalitat dels desenvolupaments en un entorn de depuració, el servidor OPC UA interactua amb la base de dades

InfluxDB mitjançant Telegraf, i la informació es visualitza en temps real amb Grafana (Figura 9.13). Aquesta configuració permet monitoritzar temperatures, tensions i potències òptiques dels transceptors, mostrant la viabilitat de la solució en entorns reals. Tot i que les proves amb el sistema complet encara estan en desenvolupament, els resultats preliminars amb les lectures internes del CPM mostren que la infraestructura de control i monitoratge funciona correctament.

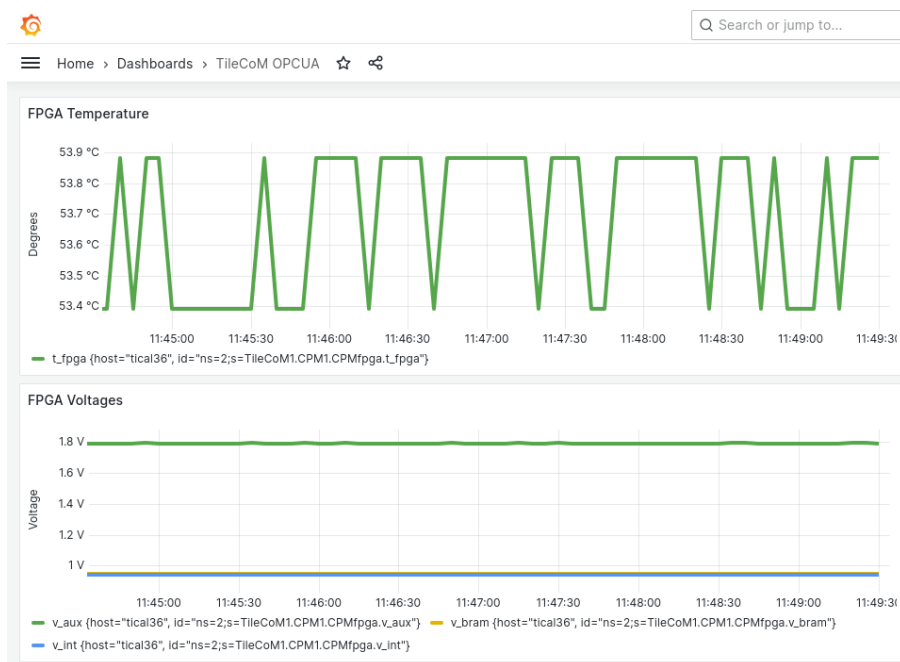


Figure 9.13: Monitoratge en temps real de la FPGA del CPM mitjançant Grafana. El gràfic superior mostra la temperatura interna de la FPGA, obtinguda a través d'OPC UA. El gràfic inferior mostra els rails de tensió auxiliar, de *BRAM* i interna de la FPGA.

## 9.4 Disseny del ATCA switch board

Per garantir la comunicació entre tots els mòduls TilePPr allotjats en una mateixa ATCA *shelf*, es desenvolupa una placa commutadora específica que

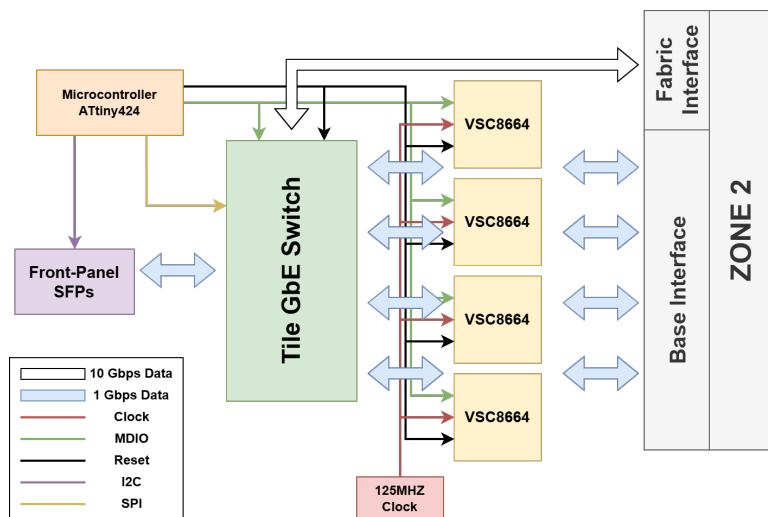


Figure 9.14: Detailed block diagram of the ATCA switch board network block design.

actua com a nucli de connexió per a la *Base Interface* de la infraestructura. Aquesta solució elimina la necessitat d'interconnexions manuals externes i minimitza la complexitat del cablejat, millorant l'eficiència i l'ordenació del sistema.

La placa integra un *switch* GbE de 16 ports, connectat a transceptors VSC8664 per a la conversió *Media Access Control* (MAC)-a-*Physical Layer* (PHY), i incorpora ports *Small Form-factor Pluggable* (SFP) al panell frontal per a la comunicació externa (Figura 9.14). Les línies de la *Fabric Interface* també es connecten al *switch*, permetent futures actualitzacions a 10 *Gigabits per second* (Gbps) si és necessari.

El disseny incorpora un concentrador USB per facilitar les tasques de depuració, amb accés frontal a diversos ports. L'alimentació s'organitza mitjançant convertidors *Direct Current to Direct Current converter* (DC-DC), un mòdul d'entrada de potència i una interfície per a IPMC, que controla l'arrencada, monitoritza els paràmetres i gestiona les alarmes del sistema corresponent al *ATCA Switch board*.



La *Printed Circuit Board* (PCB) es dissenya seguint l'estàndard ATCA, amb una distribució de 10 capes: quatre per a senyal, dues per als plans d'alimentació i quatre per a plans de terra. Les línies de transmissió es calculen i validen mitjançant models teòrics i l'eina d'impedància integrada en KiCAD.

Després de la fabricació, s'avalua la qualitat de les línies mitjançant mesures *Time Domain Reflectometry* (TDR), que mostren una impedància pròxima a 80 ohms en les traces més llargues referents al GbE, degut a l'absència de control d'impedància durant la producció. Tot i això, el comportament del sistema es manté dins dels marges operatius. La Figura 9.15 mostra la PCB completament muntada.

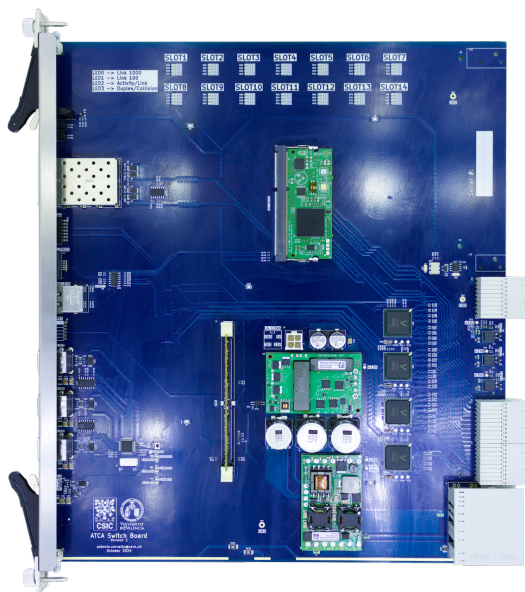


Figure 9.15: ATCA switch board fully assembled.

En les proves de rendiment, la placa es instal·lada en una ATCA *shelf* on es mesura el trànsit de dades amb la ferrament *iperf3*, que confirma una taxa de transferència pròxima a 1 Gbps sense pèrdues de dades (Figura 9.16). També es realitzen proves de llarga durada amb èxit, validant l'estabilitat i fiabilitat del disseny en condicions de càrrega sostinguda.

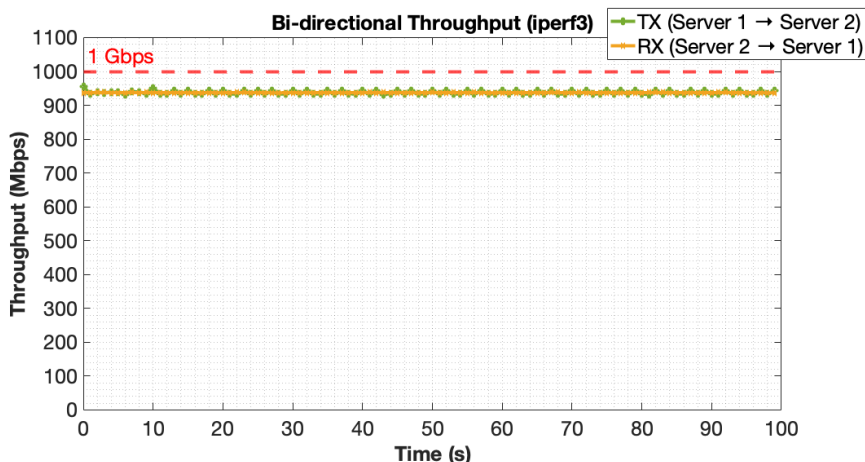


Figure 9.16: Resultats de la prova de rendiment utilitzant l'eina *iperf3*, mostrant la transmissió i recepció simultànies. El gràfic demostra que el sistema assoleix un ample de banda pròxim a l'objectiu dissenyat d'1 Gbps.

## 9.5 Integració dels desenvolupaments

### 9.5.1 Testbeam

Durant diverses campanyes de testbeam a la línia H8 del SPS de CERN, es valida el nou sistema de lectura i adquisició de dades del TileCal, comparant-lo amb l'electrònica llegada. Es col·loquen cinc mòduls sobre una taula mòbil, amb tres d'ells instrumentats amb electrònica tradicional i dos amb el sistema actualitzat, incloent targetes FENICS, *MainBoard* i *DaughterBoard*. Cada mòdul està connectat a sistemes de potència d'alta i baixa tensió, i controlat mitjançant DCS a través de *Controller Area Network Bus* (CANBus).

Els mòduls llegats es connecten a una configuració reduïda basada en RODs, mentre que els mòduls actualitzats utilitzen inicialment el TilePPr Demonstrator i posteriorment la placa CPM, la qual permet transmetre dades simultàniament als sistemes llegat i FELIX. El sistema de TTC, basat en ALTI, proporciona la configuració i el senyal de rellotge per a tota l'electrònica.

Al llarg de la línia de feix (Figura 9.17), es disposen detectors com *Delay Wire Chamber* (DWC), *Muon Hodoscope* (MH), *Cherenkov Counters* (CC) i

diversos centellejadors, que permeten determinar la posició del feix, identificar partícules i generar el senyal de *trigger*. El sistema de *trigger* combina senyals de diversos centellejadors, transmet la senyal de L1A al sistema i coordina la lectura de dades.

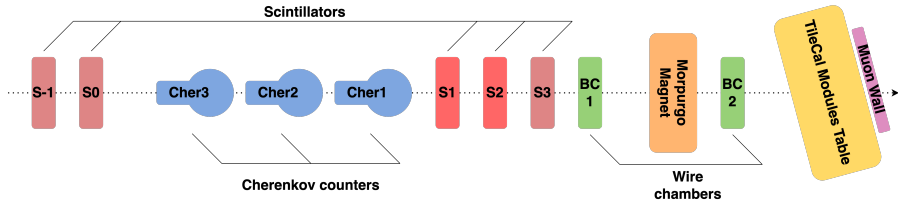


Figure 9.17: Esquema dels elements del feix al *testbeam*. La línia discontinua representa la trajectòria del feix.

La lectura de dades es realitza en paral·lel mitjançant els formats llegit i FELIX, amb una validació automàtica de paquets mitjançant SWROD. Les dades es combinen en un arxiu *RAW* per a la reconstrucció posterior. A més, es recullen dades de l'integrador de manera contínua sense interferir en l'adquisició principal.

El sistema de monitoratge *Data Quality Monitoring* (DQM) permet una verificació visual i en temps real de l'estat del sistema, amb gràfics i alertes codificades per colors. També s'utilitza el *TileEventViewer* per inspeccionar individualment els paquets i comprovar la seva decodificació, incloent les noves estructures de dades del sistema FELIX.

Els resultats mostren una adquisició estable i precisa ambdós formats de lectura, i la comparació entre sistemes demostra una gran coherència. S'hi realitzen validacions amb dades de calibració de Cessi i mesures de polsos d'alta i baixa amplificació (Figura 9.18 i Figura 9.19). A més, a la Figura 9.20 es mostra un anàlisi de correlació de soroll que evidencia una reducció significativa del soroll coherent en el sistema actualitzat. Aquest comportament confirma la millora de la integritat de senyal i el bon aïllament dels canals del sistema de lectura de la Fase-II.

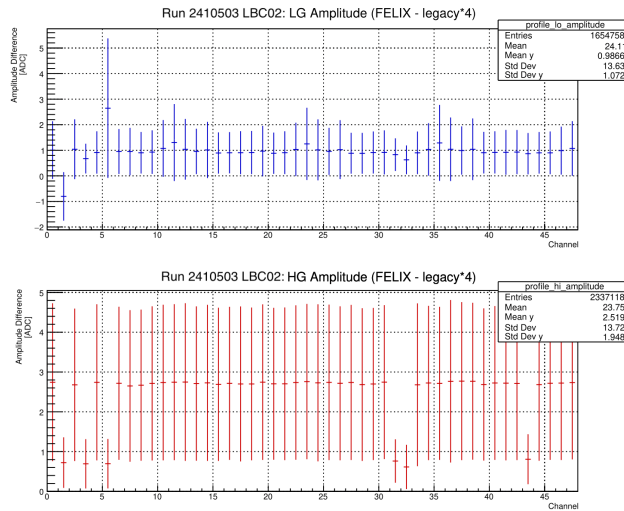


Figure 9.18: Comparació de les diferències d'amplitud en ganancia baixa (superior) i ganancia alta (inferior) entre les lectures del FELIX i les del sistema actual durant una execució de pedestal (Run Number 2410503) en el mòdul d'actualització. Els valors més baixos indiquen canals no instrumentats o sorollosos.

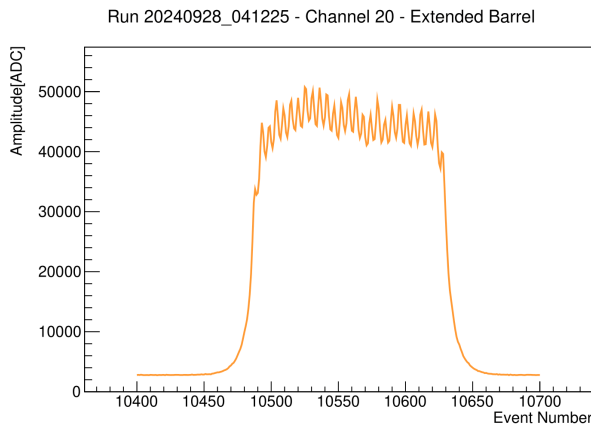


Figure 9.19: Gràfic de la lectura de l'integrador obtinguda mitjançant FELIX, mostrant els valors de ADC mesurats durant el pas de la càpsula de Cessi per el canal 20 (cèl·lula A14-R) del barril estès, durant la campanya del *testbeam* del setembre de 2024.

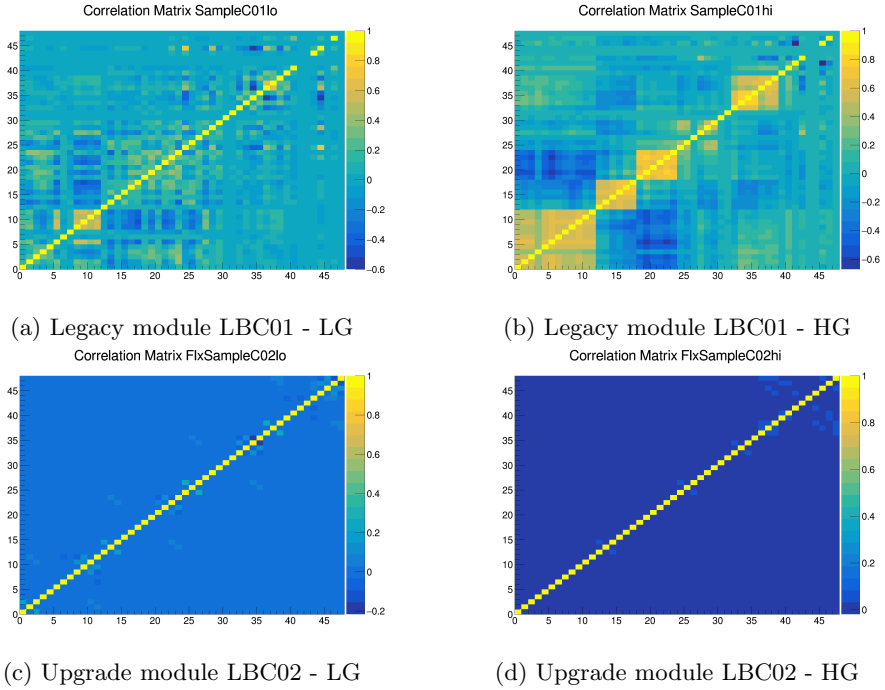


Figure 9.20: Comparació de la correlació de soroll entre un mòdul antic amb lectura antiga i un mòdul actualitzat amb lectura mitjançant FELIX, obtinguda a partir d'una execució de pedestal (Run Number 2420799).

### 9.5.2 ATLAS

S'implementa un sistema de lectura basat en FELIX al mòdul Demonstrator del detector ATLAS, amb l'objectiu de validar l'arquitectura proposada per a la Fase-II. El mòdul Demonstrator, introduït en el mòdul LBA14 el juliol de 2019 i integrat completament el maig de 2020, ha recollit dades de manera continuada utilitzant els ROD del sistema llegat com a sistema principal de lectura, funcionant de forma ininterrompuda durant tota la presa de dades del Run 3. El mòdul inclou tots els components nous del sistema de lectura i conserva la capacitat de generar senyals de *trigger* analògics compatibles amb l'actual sistema de L1Calo. Es configura per funcionar en paral·lel tant amb el sistema llegat com amb el sistema FELIX, cosa que permet comparacions i

una validació funcional completa.

La infraestructura de lectura es desplega a la sala USA15, on s'instal·len els servidors FELIX i SWROD, juntament amb el cablejat de fibra òptica necessari per a establir les connexions entre els servidors i la placa CPM dins del TilePPr. Els enllaços funcionen en mode *GigaBit Transceiver* (GBT) a 4.8 Gbps, un entorn provat i estable per a la lectura continua de dades.

Per a validar el sistema, es duen a terme proves en la partició Standalone de TileCal. En la partició Standalone, el sistema SWROD s'integra amb un consumidor de fragments especialitzat que permet combinar les dades de lectura amb altres mòduls mitjançant el mòdul REB.

S'implementa un doble flux de lectura que envia simultàniament les dades cap al sistema llegat i al nou sistema basat en FELIX. Aquesta configuració proporciona redundància, possibilita comparacions precises entre sistemes, i permet aprofitar els avantatges del nou format.

Actualment, el sistema demostra una integració funcional completa dins del marc de TDAQ, i es preveu continuar amb l'adquisició de dades de calibració i operació rutinària per validar el rendiment del sistema en condicions reals.

## 9.6 Conclusions

Aquesta tesi s'ha desenvolupat en el marc de l'actualització del Calorímetre Tile de l'experiment ATLAS, de cara a l'era del High-Luminosity Large Hadron Collider (HL-LHC). L'objectiu principal ha sigut el disseny, implementació i validació de nous sistemes de lectura, control i adquisició de dades que siguin capaços de respondre als requisits més exigents en amplada de banda, tolerància a la radiació i precisió en la temporització imposats per les condicions del HL-LHC.

Una de les principals contribucions d'aquest treball ha sigut el desenvolupament i integració d'una cadena moderna de TDAQ per a TileCal, mitjançant la incorporació dels sistemes FELIX i SWROD. Aquest nou esquema substitueix

amb èxit el *hardware* heretat, oferint una alternativa escalable i basada en *software*, compatible amb comunicacions d'alta velocitat.

S'han desenvolupat complements específics per al SWROD que permeten la integració transparent de dades procedents tant de FELIX com del sistema llegat. Aquesta estratègia facilita la unificació de dades de campanyes de testbeam i de la partició autònoma de Tile en un únic fitxer, simplificant-ne l'anàlisi posterior.

També s'ha proposat una nova metodologia de lectura per a l'integrador basada en FELIX, recolzada per una biblioteca pròpia que permet extreure les dades dels mòduls CPM i emmagatzemar-les en disc per a la seua anàlisi fora de línia. Es van desenvolupar dues aplicacions amb aquesta biblioteca: una orientada a l'ús autònom (com per exemple en la calibració amb Cesi) i una altra integrada en la partició TDAQ, operant segons l'esquema de control FSM.

Paral·lelament, la tesi descriu el desenvolupament d'aplicacions per al Tile-CoM, un mòdul compacte basat en System-on-Chip per al control i monitoratge de l'electrònica dins i fora del detector. A través de diverses iteracions i fases de depuració, s'han generat imatges funcionals dels sistemes PetaLinux i AlmaLinux, incloent-hi modificacions al FSBL per garantir una correcta inicialització de xarxa. S'ha establert una infraestructura automatitzada amb Git-Lab CI/CD per assegurar control de versions, reproductibilitat i eficiència en el desenvolupament. La integració dels protocols OPC UA i IPbus ha proporcionat una interfície robusta per al control remot i el monitoratge, demostrant l'estat de maduresa del TileCoM per a la seua futura implementació.

Per a permetre la comunicació entre tots els mòduls TilePPr dins d'una shelf ATCA, també s'ha dissenyat una placa commutadora personalitzada (ATCA *Switch Board*). Les proves de validació amb eines com *iperf3* han confirmat la capacitat del sistema per mantindre transmissions de 1 Gbps sense errors en tots els canals.

Tots aquests sistemes han estat validats amb èxit en diverses campanyes

de testbeam i posteriorment integrats en el mòdul demostrador d'ATLAS, on el seu funcionament s'ha verificat en condicions reals d'operació.

Aquest treball representa una contribució rellevant en la modernització de l'electrònica i el sistema de lectura de TileCal. Les eines, metodologies i infraestructures desenvolupades tindran un paper clau en assegurar el rendiment, fiabilitat i flexibilitat del sistema durant l'operació del HL-LHC.



# List of Acronyms

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <b>ACBB</b>   | ATCA Carrier BaseBoard                                    |
| <b>ADC</b>    | Analog-to-Digital Converter                               |
| <b>AFP</b>    | ATLAS Forward Proton                                      |
| <b>ALFA</b>   | Absolute Luminosity For ATLAS                             |
| <b>ALICE</b>  | A Large Ion Collider Experiment                           |
| <b>ALTI</b>   | ATLAS Local Trigger Interface                             |
| <b>AMC</b>    | Advanced Mezzanine Card                                   |
| <b>AM</b>     | Access Manager                                            |
| <b>AMD</b>    | Advanced Micro Devices                                    |
| <b>APU</b>    | Application Processing Unit                               |
| <b>ARM</b>    | Advanced RISC (Reduced Instruction Set Computer) Machines |
| <b>ASIC</b>   | Application-Specific Integrated Circuit                   |
| <b>ATCA</b>   | Advanced Telecommunications Computing Architecture        |
| <b>ATLAS</b>  | A Toroidal LHC ApparatuS                                  |
| <b>AXI</b>    | Advanced eXtensible Interface                             |
| <b>BC</b>     | Bunch Crossing                                            |
| <b>BCID</b>   | Bunch Crossing Identifier                                 |
| <b>BCR</b>    | Bunch Crossing Reset                                      |
| <b>CANBus</b> | Controller Area Network Bus                               |
| <b>CC</b>     | Cherenkov Counters                                        |

|                |                                                                                           |
|----------------|-------------------------------------------------------------------------------------------|
| <b>CERN</b>    | European Organization for Nuclear Research (Conseil Européen pour la Recherche Nucléaire) |
| <b>CI/CD</b>   | Continuous Integration / Continuous Deployment                                            |
| <b>CIS</b>     | Charge Injection System                                                                   |
| <b>CMS</b>     | Compact Muon Solenoid                                                                     |
| <b>COTS</b>    | Commercial Off-The-Shelf                                                                  |
| <b>CPU</b>     | Central Processing Unit                                                                   |
| <b>CPM</b>     | Compact Processing Module                                                                 |
| <b>CRC</b>     | Cyclic Redundancy Check                                                                   |
| <b>CSU</b>     | Configuration Security Unit                                                               |
| <b>CTP</b>     | Central Trigger Processor                                                                 |
| <b>DAC</b>     | Digital-to-Analog Converter                                                               |
| <b>DAQ</b>     | Data Acquisition                                                                          |
| <b>daq2dcs</b> | DAQ to DCS communication system                                                           |
| <b>DC-DC</b>   | Direct Current to Direct Current converter                                                |
| <b>DCS</b>     | Detector Control System                                                                   |
| <b>DDR4</b>    | Double Data Rate 4                                                                        |
| <b>DMA</b>     | Direct Memory Access                                                                      |
| <b>DQM</b>     | Data Quality Monitoring                                                                   |
| <b>DSP</b>     | Digital Signal Processor                                                                  |
| <b>DTS</b>     | Device Tree Source                                                                        |
| <b>DTB</b>     | Device Tree Blob                                                                          |
| <b>DWC</b>     | Delay Wire Chamber                                                                        |
| <b>EBA</b>     | Extended Barrel A                                                                         |
| <b>EB</b>      | Extended Barrel                                                                           |
| <b>EBC</b>     | Extended Barrel C                                                                         |
| <b>ECR</b>     | Event Counter Reset                                                                       |
| <b>EF</b>      | Event Filter                                                                              |

|                |                                                                                   |
|----------------|-----------------------------------------------------------------------------------|
| <b>ELMB</b>    | Embedded Local Monitor Board                                                      |
| <b>ELMB-MB</b> | ELMB-motherboard                                                                  |
| <b>eMMC</b>    | embedded MultiMediaCard                                                           |
| <b>EMCI</b>    | Embedded Monitoring and Control Interfaces                                        |
| <b>EMP</b>     | Embedded Monitoring Processor                                                     |
| <b>FASER</b>   | Forward Search Experiment                                                         |
| <b>FELIX</b>   | Front-End LInk eXchange                                                           |
| <b>FENICS</b>  | Front-End board for the New Infrastructure with Calibration and<br>Signal Shaping |
| <b>FEX</b>     | Feature Extractor                                                                 |
| <b>FIFO</b>    | First In, First Out                                                               |
| <b>FMC</b>     | FPGA Mezzanine Card                                                               |
| <b>FPGA</b>    | Field-Programmable Gate Array                                                     |
| <b>FR4</b>     | Flame Retardant 4                                                                 |
| <b>FRU</b>     | Field Replaceable Unit                                                            |
| <b>FSM</b>     | Finite State Machine                                                              |
| <b>FSBL</b>    | First Stage Boot Loader                                                           |
| <b>GbE</b>     | Gigabit Ethernet                                                                  |
| <b>Gbps</b>    | Gigabits per second                                                               |
| <b>GBT</b>     | GigaBit Transceiver                                                               |
| <b>GND</b>     | Ground                                                                            |
| <b>GPIO</b>    | General Purpose Input/Output                                                      |
| <b>GTR</b>     | Gigabit Transceiver                                                               |
| <b>GUI</b>     | Graphical User Interface                                                          |
| <b>HG</b>      | High Gain                                                                         |
| <b>HEP</b>     | High Energy Physics                                                               |
| <b>HL-LHC</b>  | High-Luminosity LHC                                                               |
| <b>HLT</b>     | High-Level Trigger                                                                |

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <b>HTT</b>      | Hardware Tracking for the Trigger                                    |
| <b>HV</b>       | High-Voltage                                                         |
| <b>HVAD</b>     | High-Voltage Active Divider                                          |
| <b>I2C</b>      | Inter-Integrated circuit                                             |
| <b>ID</b>       | Inner Detector                                                       |
| <b>IFIC</b>     | Institut de Física Corpuscular                                       |
| <b>IGUI</b>     | Integrated Graphical User Interface                                  |
| <b>ILANA</b>    | Interface for the LAsEr system to the New Acquisition infrastructure |
| <b>IP</b>       | Internet Protocol                                                    |
| <b>IP block</b> | Intellectual Property block                                          |
| <b>IPbus</b>    | Internet Protocol bus                                                |
| <b>IPC</b>      | Inter-Process Communication                                          |
| <b>IPMB</b>     | Intelligent Platform Management Bus                                  |
| <b>IPMC</b>     | Intelligent Platform Management Controller                           |
| <b>IS</b>       | Information Services                                                 |
| <b>ITk</b>      | Inner Tracker                                                        |
| <b>JSON</b>     | JavaScript Object Notation                                           |
| <b>JTAG</b>     | Joint Test Action Group                                              |
| <b>L0</b>       | Level-0 (Trigger System)                                             |
| <b>L0A</b>      | Level-0 Accept signal                                                |
| <b>L0Calo</b>   | Level-0 Calorimeter                                                  |
| <b>L0Muon</b>   | Level-0 Muon                                                         |
| <b>L1</b>       | Level-1 (First-level trigger)                                        |
| <b>L1A</b>      | Level-1 Accept signal                                                |
| <b>L1Calo</b>   | Level-1 Calorimeter                                                  |
| <b>L1ID</b>     | Level-1 IDentifier                                                   |
| <b>L1Muon</b>   | Level-1 Muon                                                         |
| <b>L1Topo</b>   | Level-1 Topological Processor                                        |

|                |                                             |
|----------------|---------------------------------------------|
| <b>LAr</b>     | Liquid Argon                                |
| <b>LASCAR</b>  | Laser Calibration                           |
| <b>LBA</b>     | Long Barrel A                               |
| <b>LB</b>      | Long Barrel                                 |
| <b>LBC</b>     | Long Barrel C                               |
| <b>LC</b>      | Lucent Connector                            |
| <b>LED</b>     | Light Emitting Diode                        |
| <b>LG</b>      | Low Gain                                    |
| <b>LHC</b>     | Large Hadron Collider                       |
| <b>LHCb</b>    | LHC beauty                                  |
| <b>LHCf</b>    | LHC forward                                 |
| <b>Linac4</b>  | Linear Accelerator 4                        |
| <b>LS2</b>     | Long Shutdown 2                             |
| <b>LS3</b>     | Long Shutdown 3                             |
| <b>LTi</b>     | Local Trigger Interface                     |
| <b>LTPI</b>    | Local Trigger Processor Interface           |
| <b>LTP</b>     | Local Trigger Processor                     |
| <b>LUCID-2</b> | LUminosity Cherenkov Integrating Detector 2 |
| <b>LV</b>      | Low-Voltage                                 |
| <b>LVDS</b>    | Low-voltage differential signaling          |
| <b>LVPS</b>    | Low-Voltage Power Supply                    |
| <b>MAC</b>     | Media Access Control                        |
| <b>MAPMT</b>   | Multi-Anode Photomultiplier Tube            |
| <b>MB</b>      | Minimum Bias                                |
| <b>Mbps</b>    | Megabits per second                         |
| <b>MBTS</b>    | Minimum Bias Trigger Scintillators          |
| <b>MDIO</b>    | Management Data Input/Output                |
| <b>MDT</b>     | Monitoring Drift Tube                       |

|                    |                                                                                          |
|--------------------|------------------------------------------------------------------------------------------|
| <b>MH</b>          | Muon Hodoscope                                                                           |
| <b>MGT</b>         | Multi-Gigabit Transceiver                                                                |
| <b>MMC</b>         | Module Management Controller                                                             |
| <b>MiniPOD</b>     | Mini Parallel Optical Device                                                             |
| <b>MoEDAL-MAPP</b> | Monopole and Exotics Detector at the LHC - MoEDAL<br>Apparatus for Penetrating Particles |
| <b>MPSoC</b>       | Multiprocessor System on Chip                                                            |
| <b>MS</b>          | Muon Spectrometer                                                                        |
| <b>MTP24</b>       | Multifiber Termination Push-on 24                                                        |
| <b>MUCTPI</b>      | Muon-to-Central-Trigger-Processor Interface                                              |
| <b>NAND</b>        | Not AND (type of flash memory)                                                           |
| <b>NIM</b>         | Nuclear Instrumentation Module                                                           |
| <b>NSW</b>         | New Small Wheel                                                                          |
| <b>OCM</b>         | On-Chip Memory                                                                           |
| <b>OKS</b>         | Object Kernel Support                                                                    |
| <b>OPC</b>         | Open Platform Communications                                                             |
| <b>OPC UA</b>      | Open Platform Communications Unified Architecture                                        |
| <b>OS</b>          | Operating System                                                                         |
| <b>PCB</b>         | Printed Circuit Board                                                                    |
| <b>PCIe</b>        | Peripheral Component Interconnect Express                                                |
| <b>PICMG</b>       | PCI Industrial Computer Manufacturers Group                                              |
| <b>PHY</b>         | Physical Layer                                                                           |
| <b>PL</b>          | Programmable Logic                                                                       |
| <b>PMG</b>         | Process ManaGer                                                                          |
| <b>PMT</b>         | PhotoMultiplier Tube                                                                     |
| <b>PMU</b>         | Power Management Unit                                                                    |
| <b>PS</b>          | Proton Synchrotron                                                                       |
| <b>PS</b>          | Processing System                                                                        |

|                |                                             |
|----------------|---------------------------------------------|
| <b>PSB</b>     | Proton Synchrotron Booster                  |
| <b>PU</b>      | Processing Unit                             |
| <b>QEMU</b>    | Quick Emulator                              |
| <b>QSPI</b>    | Quad Serial Peripheral Interface            |
| <b>RAM</b>     | Random-Access Memory                        |
| <b>RC</b>      | Run Control                                 |
| <b>RDB</b>     | Remote DataBase                             |
| <b>RDMA</b>    | Remote Direct Memory Access                 |
| <b>REB</b>     | ROS Event Builder                           |
| <b>RJ-45</b>   | Registered Jack 45                          |
| <b>RM</b>      | Resource Manager                            |
| <b>ROB</b>     | ReadOut Buffer                              |
| <b>RoCE</b>    | RDMA over Converged Ethernet                |
| <b>ROD</b>     | Read Out Driver                             |
| <b>RODRCD</b>  | ROD ROD Crate DAQ                           |
| <b>RoIs</b>    | Regions-of-Interest                         |
| <b>ROS</b>     | ReadOut System                              |
| <b>RPC</b>     | Resistive Plate Chamber                     |
| <b>RPM</b>     | Red Hat Package Manager                     |
| <b>RPU</b>     | Real-time Processing Unit                   |
| <b>RTM</b>     | Rear Transition Module                      |
| <b>RTOS</b>    | Real-Time Operating System                  |
| <b>SBC</b>     | Single Board Computer                       |
| <b>SD</b>      | Secure Digital                              |
| <b>SFP</b>     | Small Form-factor Pluggable                 |
| <b>SHAFT</b>   | SHared A Few Triggers                       |
| <b>SIN</b>     | Sensor based in INductance                  |
| <b>SND@LHC</b> | Scattering and Neutrino Detector at the LHC |

|                |                                                          |
|----------------|----------------------------------------------------------|
| <b>SoC</b>     | System-on-Chip                                           |
| <b>SO-DIMM</b> | Small Outline - Dual In-line Memory Module               |
| <b>SPI</b>     | Serial Peripheral Interface                              |
| <b>SPS</b>     | Super Proton Synchrotron                                 |
| <b>SSBL</b>    | Second Stage Boot Loader                                 |
| <b>ST</b>      | Straight Tip                                             |
| <b>sTGC</b>    | small-strip Thin Gap Chamber                             |
| <b>SWROD</b>   | SoftWare ReadOut Driver                                  |
| <b>TDAQ</b>    | Trigger and Data Acquisition                             |
| <b>TDAQi</b>   | Trigger and Data AcQuisition interface                   |
| <b>TBM</b>     | Trigger and Busy Module                                  |
| <b>TDC</b>     | Time-to-Digital Converter                                |
| <b>TGC</b>     | Thin Gap Chamber                                         |
| <b>TF-A</b>    | Trusted Firmware-A                                       |
| <b>TileCal</b> | Tile Calorimeter                                         |
| <b>TileCoM</b> | Tile Computer-on-Module                                  |
| <b>TileDMU</b> | Tile Data Management Unit                                |
| <b>TilePPr</b> | Tile PreProcessor                                        |
| <b>TMDB</b>    | Tile Muon Digitizer Board                                |
| <b>TMDBRCD</b> | TMDB ROD Crate DAQ                                       |
| <b>TDR</b>     | Time Domain Reflectometry                                |
| <b>ToF</b>     | Time of Flight                                           |
| <b>TOTEM</b>   | TOTal, Elastic and diffractive cross-section Measurement |
| <b>TCP</b>     | Transmission Control Protocol                            |
| <b>TCP/IP</b>  | Transmission Control Protocol/Internet Protocol          |
| <b>TTC</b>     | Trigger, Timing, and Control                             |
| <b>TTCex</b>   | TTC Emitter                                              |
| <b>TTCoc</b>   | TTC Optical Coupler                                      |



|               |                                                   |
|---------------|---------------------------------------------------|
| <b>TTCpr</b>  | TTC Receiver in PCIe Mezzanine Card               |
| <b>TTCrx</b>  | TTC receiver                                      |
| <b>TTCvi</b>  | TTC VMEbus Interface                              |
| <b>TTCRCD</b> | TTC ROD Crate DAQ                                 |
| <b>UART</b>   | Universal Asynchronous Receiver/Transmitter       |
| <b>USA15</b>  | Underground Service Area 15 (ATLAS Counting Room) |
| <b>USB</b>    | Universal Serial Bus                              |
| <b>VME</b>    | Versa Module Eurocard                             |
| <b>WLS</b>    | WaveLength Shifting                               |
| <b>XML</b>    | eXtensible Markup Language                        |
| <b>YETS</b>   | Year-End Technical Stop                           |
| <b>ZDC</b>    | Zero Degree Calorimeter                           |



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